Vellore – 632014, Tamil Nadu, India

SCHOOL OF ELECTRICAL ENGINEERING

WINTER SEMESTER 2023-2024

CAT-II

SLOT: C1+TC1

Programme Name & Branch : B.Tech(EIE & EEE) Course Code: BEEE206L
Course Name : Digital Electronics
Faculty Members : R.Santhakumar Class Number(s): VL2023240502739

Date of the Examination : 03-04-2024
Duration : 90 minutes **Max. Marks : 50**

General instruction(s): Answer all the questions

Q. No	Question	Mark	CO	BL
1.	Draw the logical diagrams for the following Boolean expressions using NAND Gate only and write Verilog code for the circuit using Gate level model. Y=A'B'+B(A+C).	10	2	BL
2.	Design a combinational circuit with three inputs, x, y and z, and the three outputs, A, B, and C. when the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. Implement the circuit using Multiplexer.	10	1	BL
3.	Convert SR flip-flop to JK, D, and T flip-flop and write Verilog program for SR flip-flop to T flip-flop conversion.	10	2	BL
4.a	Design a counter with T-Flip Flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. show that when 2 and 5 are taken to be don't care conditions, the counter may not operate properly	8	3	BL
4.b	The content of a 4 bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift?	2	3	BL
5.	Design sequential circuit to detect the sequence 10110 from received binary sequence using mealy machine.	10	4	BL

Question Paper Setter Moderator