24MIS0205

VIT
Vellore Institute of Technology

Slot :C2

School of Computer Science Engineering and Information Systems

Winter Semester 2024-2025

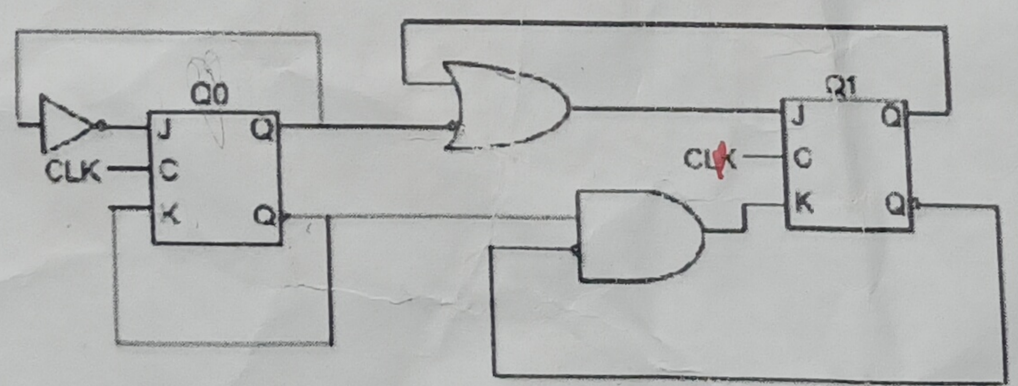
Continuous Assessment Test – II

Programme Name & Branch: M.Tech (Software Engineering)
Course Name & code: ISWE201L Digital Logic and Microprocessor
Class Number (s): VL2024250503339, VL2024250503345, VL2024250503343 VL2024250503341
Faculty Name (s): Prof. SUGANYA P , Prof.SENTHILKUMAR , Prof. SUMATHI D, Prof.USHAPREETHI P

Exam Duration: 90 Min. **Maximum Marks: 50**

Q.No.	Question	Max Marks	CO	BL
1.	Design a sequential circuit for the following state table using T Flip Flop. Identify the model and draw the state diagram also.	10	CO4	BL6
2.	a. Convert the following gray value to binary, and find the excess-3 value for the identified binary value. (3 marks) 110011011101 b. Analyze the given circuit and find its state table and state diagram. (7 marks)	10	CO3	BL4

Present State A	Present State B	Input x	Next State A	Next State B	Output y
0	0	0	1	0	0
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	0
1	1	0	0	1	1
1	1	1	1	0	1

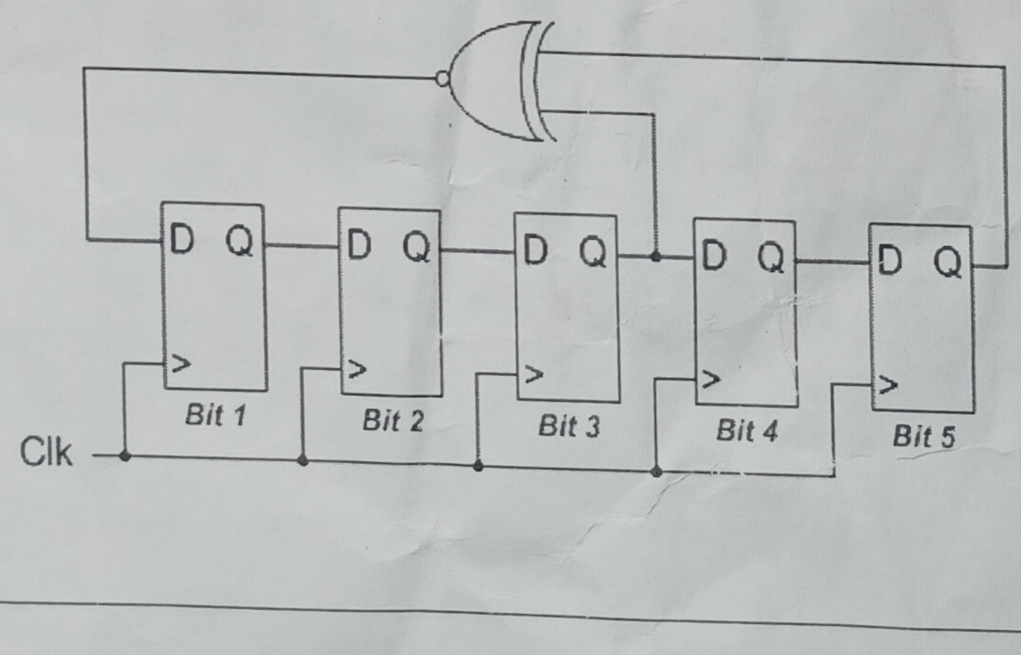


3.	a. Draw the state diagram for the following excitation table (5 marks).	10	CO3	BL3

Q(t)	Q(t+1)	X	Y
00	00	0	0
00	01	0	1
00	10	1	0
00	11	1	1
01	00	1	1
01	01	1	0
01	10	0	1
01	11	0	0
10	00	0	0
10	01	0	1
10	10	1	1
10	11	1	0
11	00	1	1
11	01	0	0

b. Derive the output of the flip flop and draw the waveform diagram by considering Q(t) is 1 during clock=0. (5 marks)

clock	J	K	Q(t+1)
1	0	0	1
2	1	0	1
3	1	1	0 1
4	1	1	1
5	1	1	0 1
6	1	0	1
7	0	0	0 1
8	0	0	1
9	0	1	0
10	1	1	1

4.	Design an asynchronous counter which counts the following sequence 7, 5, 3, 2, 1, 7, …. using D flip flops.	10	CO3	BL6
5.	Tabulate all the states for the given shift register with initial state 11001 until it reaches the same initial state again and draw the timing diagram for 6 clock cycles. 	10	CO4	BL3