School of Electronics Engineering

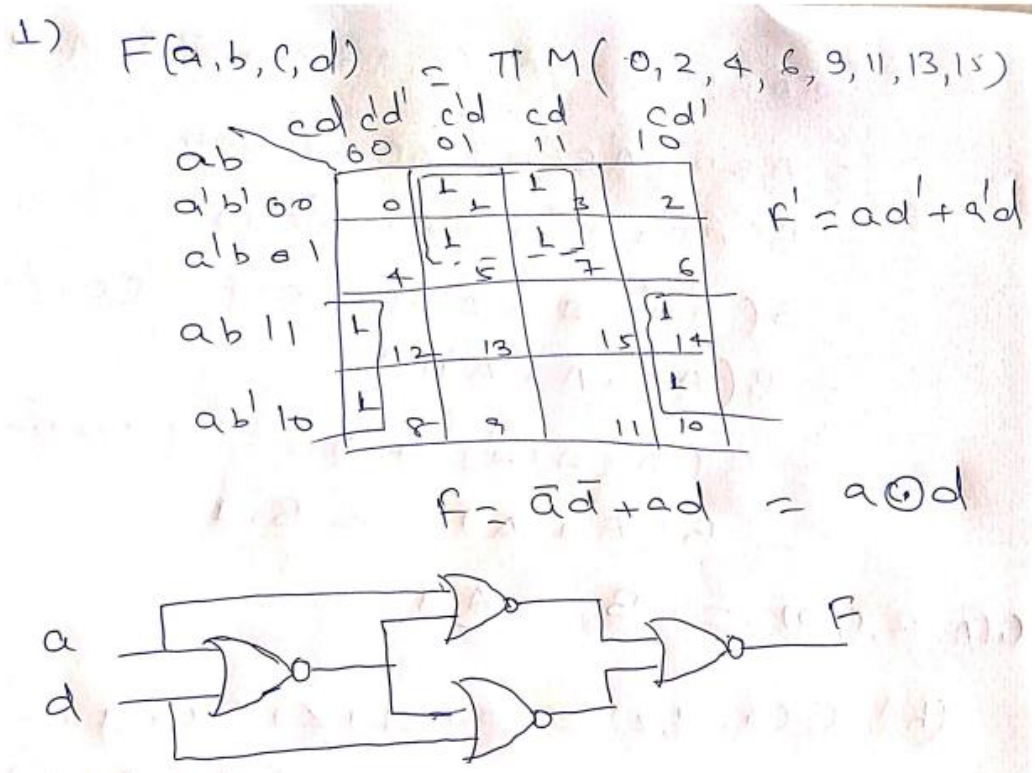
FALL Semester 2024-25

Continuous Assessment Test - I

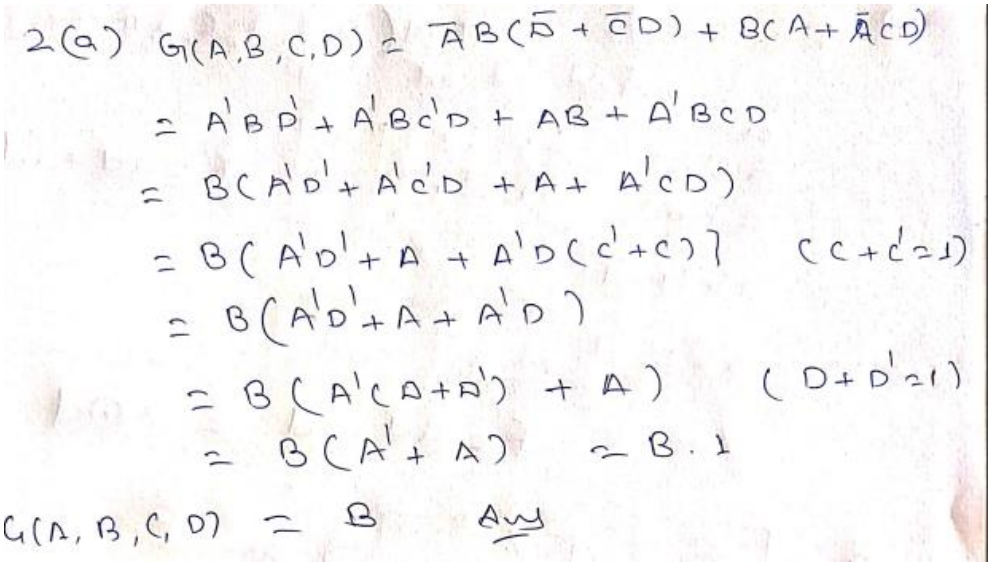
Programme : B.Tech (CSE) Course Name : Digital System Design

Course Code : BECE102L Slot : E2+TE2

Max 50 Marks

Q.No	Question	Max Marks	CO	BL
1	Simplify the Boolean function $F\ (a,\ b,\ c,\ d)$ = πM (0, 2,4,6,9,11,13,15) using K-map method and draw the logical diagram using two input NOR gates only. **Solution**:  	10	CO1	BL3
2	Reduce the following Boolean function "G" to minimum number of literals by Boolean laws/postulates/theorems and draw the logical circuit diagram with the help of basic gates. (a) $G(A,B,C,D) = \bar{A}B(\bar{D} + \bar{C}D) + B(A + \bar{A}CD)$ (b) $G(X,Y,Z) = (X + Y + Z)(X + Y + \bar{Z})\ (\bar{X} + Y + \bar{Z})$ (**Note**: Please do not use K-MAP method to solve this problem)	10	CO1	BL3

Solution:



$2(a)\ G(A,B,C,D) = \bar{A}B(\bar{D} + \bar{C}D) + B(A + \bar{A}CD)$

$= A'BD' + A'BC'D + AB + A'BCD$

$= B(A'D' + A'C'D + A + A'CD)$

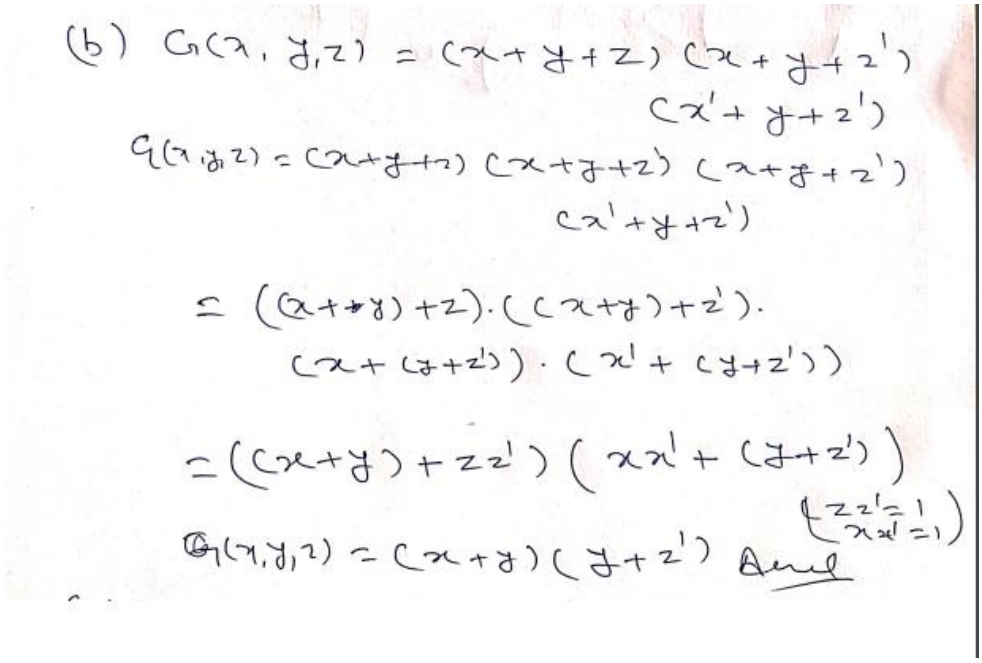
$= B(A'D' + A + A'D(C' + C))$ $(C + C' = 1)$

$= B(A'D' + A + A'D)$

$= B(A'(D + D') + A)$ $(D + D' = 1)$

$= B(A' + A) = B \cdot 1$

$G(A, B, C, D) = B$ Ans



(b) $G(x, y, z) = (x + y + z)(x + y + z')(x' + y + z')$

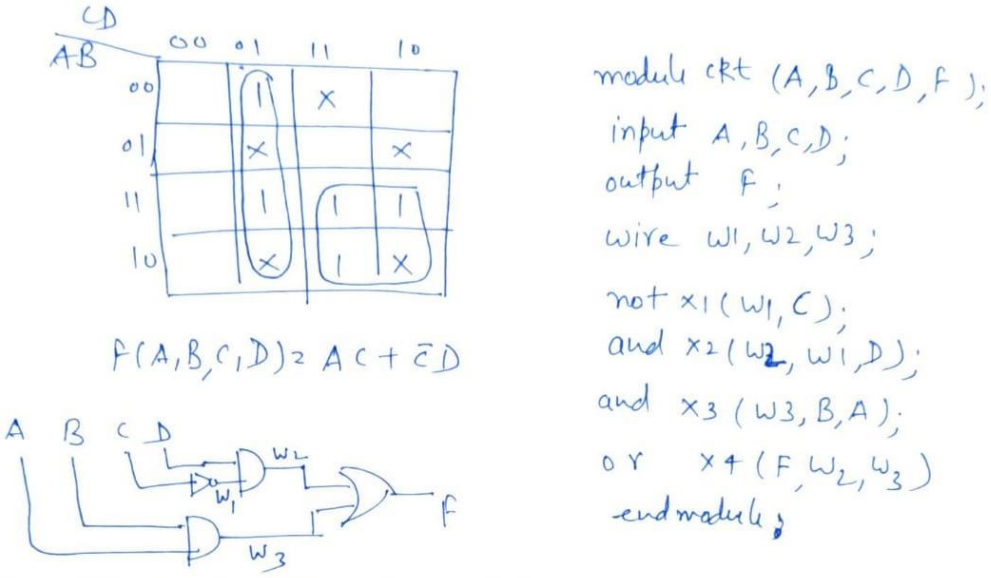
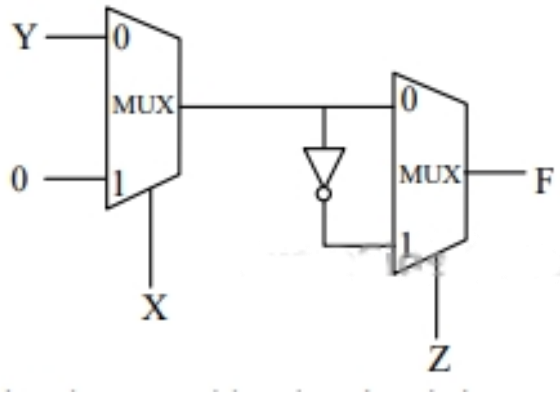
$G(x, y, z) = (x+y+z)(x+y+z')(x+y+z')(x'+y+z')$

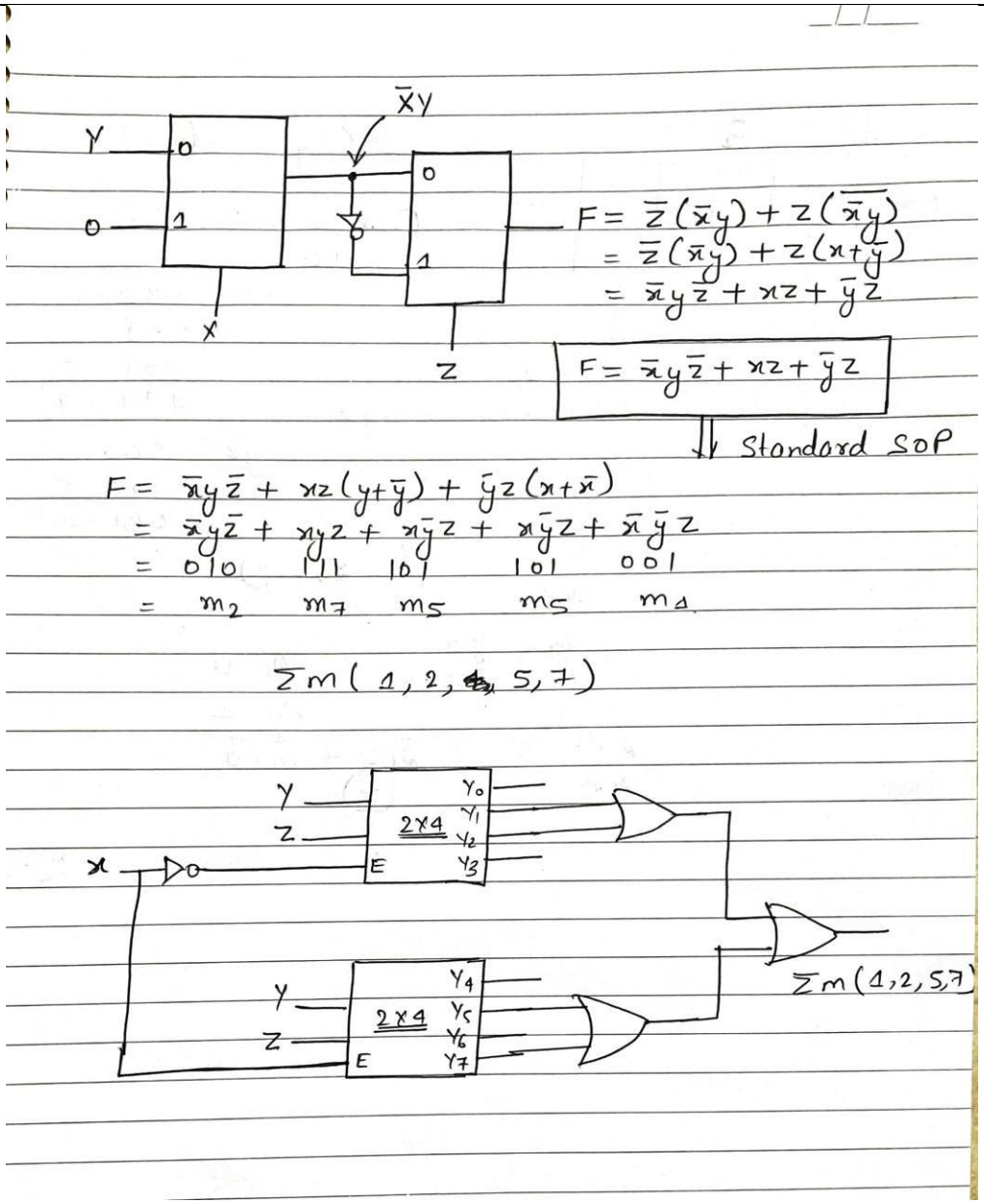
$= ((x+y)+z)\cdot((x+y)+z')\cdot(x + (y+z'))\cdot(x' + (y+z'))$

$= ((x+y) + zz')(xx' + (y+z'))$ $(zz' = 1,\ xx' = 1)$

$G(x, y, z) = (x + y)(y + z')$ Ans

3	(a) Find out errors in the following Verilog program: module 1_design (X, Y, Z); Input (X, Y); output z; assign Z = X^Y; endmodule **Solution**: Module name should not be start from a number (module 1) Input should be input output z Should be output Z	3 + 7	CO2	BL3

	(b) Develop a Verilog code for the given function "F" using structural modelling. $F(A,B,C,D) = \sum m(1,11,13,14,15) + \sum d(3,5,6,9,10)$. **Solution**:  			
4	Identify the given Boolean function (F) represented in terms of multiplexer and implement the function (F) using 2 to 4 decoder logic.  **Solution**:	10	CO3	BL3



5	Design a combinational circuit with least number of logic gates which takes input from 0 to 9 and provides output = input + 4. Write the Verilog code for designed combinational circuit in data flow modelling. **Solution** :	10	CO3	BL3

Input				Output			
A	B	C	D	P	Q	R	S
0	0	0	0	0	1	0	0
0	0	0	1	0	1	0	1
0	0	1	0	0	1	1	0
0	0	1	1	0	1	1	1
0	1	0	0	1	0	0	0
0	1	0	1	1	0	0	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	1	1
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	D	D	D	D
1	0	1	1	D	D	D	D
1	1	0	0	D	D	D	D

1	1	0	1	D	D	D	D
1	1	1	0	D	D	D	D
1	1	1	1	D	D	D	D

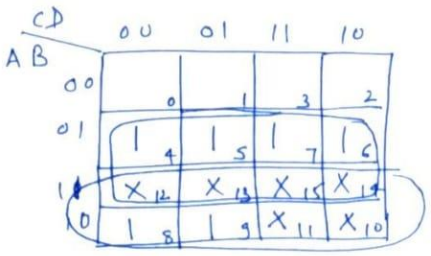
$P = \Sigma m(4,5,6,7,8,9) + \Sigma d(10,11,12,13,14,15)$

$Q = \Sigma m(0,1,2,3,8,9) + \Sigma d(10,11,12,13,14,15)$

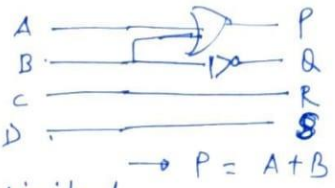
$R = \Sigma m(2,3,6,7) + \Sigma d(10,11,12,13,14,15)$

$S = \Sigma m(1,3,5,7,9) + \Sigma d(10,11,12,13,14,15)$

P =



$P = B + A$



$\rightarrow P = A + B$

Similarly

$\rightarrow Q = \overline{B}$

$R = C$

$S = D$

```
module Circuit(A,B,C,D,P,Q,R,S);
  input A,B,C,D;
  output P,Q,R,S;
  assign P=A|B, Q=~B, R=C, S=D;
  endmodule
```