



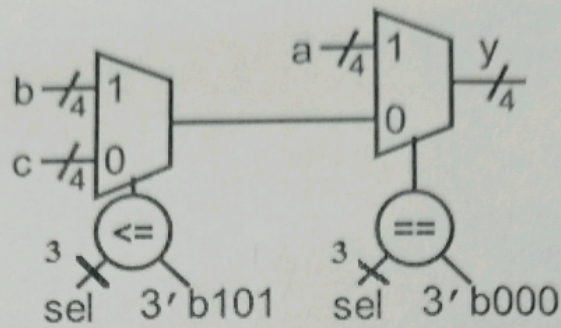
Vellore – 632014, Tamil Nadu, India
SCHOOL OF ELECTRICAL ENGINEERING
FALL SEMESTER 2024-2025
CAT-II

Programme: B.Tech	Branch: BVD	Course code: BECE102L
Course Name: Digital System Design		Date: 19/10/2024
Class Nbr: VL2024250104055	Max Marks: 50	Duration: 90 mins
Faculty name(s): Dr S.Sridevi		

General instruction(s): 1. Answer ALL

Q. No	Question	Mark
1.	<p>A bank has 4 locks with a key for each lock. Each key is owned by a different person (A,B,C,D). In order to open the vault door at least two people must insert their keys into the assigned locks at the same time. The manager (A) can open the lock alone. The signal lines (A,B,C,D) are 1 if the key is inserted into locks 1,2,3,4 respectively</p> <p>i) From the truth table, identify the min-terms for the digital locking system [3]</p> <p>ii) Implement the above function using a 4x1 Multiplexer with A and C as the select lines and B and D as the inputs. [7]</p>	10
2.	<p>A combinational circuit is specified by the following three Boolean equations.</p> $F1 = xy + \bar{x}\bar{y}\bar{z}$ $F2 = x\bar{y}\bar{z} + yz$ $F3 = \bar{x}y + \bar{y}z + xy$ <p>Implement the circuit with a decoder with active low outputs. You can use appropriate logic gates externally along with the decoder. (Note: Internal gate level diagram of the decoder is not required).</p>	10
3	Write a verilog HDL for the given circuit using behavioral style of	10

modeling



4. a) A microprocessor is associated with peripheral devices such as the disk drive, scanner, mouse and printer etc... But the microprocessor can only serve one peripheral device at a time so needs a controller that connects always an active and highly preferable peripheral device with it. Design such controller which facilitates to connect the microprocessor with the peripherals according to their priority.

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S.No	Peripheral device	Priority order
1	Key board	3
2	mouse	2
3	Parallel printer	4
4	System timer	1

- b) Write behavioural Verilog Code for the above circuit.

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5. Design a synchronous counter implemented using T-type Flip-Flops has a mode control input M. When $M = 1$, the counter output sequence represented in decimal form is 0, 1, 2, 3, 4, 5, 6, 7, and repeat. When $M = 0$, the counter output is 0. The Flip-Flop outputs are {ABC} where C represents the least significant bit of the counter output. Draw the circuit diagram

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