VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING

Fall Semester 2024-2025

Continuous Assessment Test – I

Programme Name & Branch: B.Tech **Slot: D1+TD1**

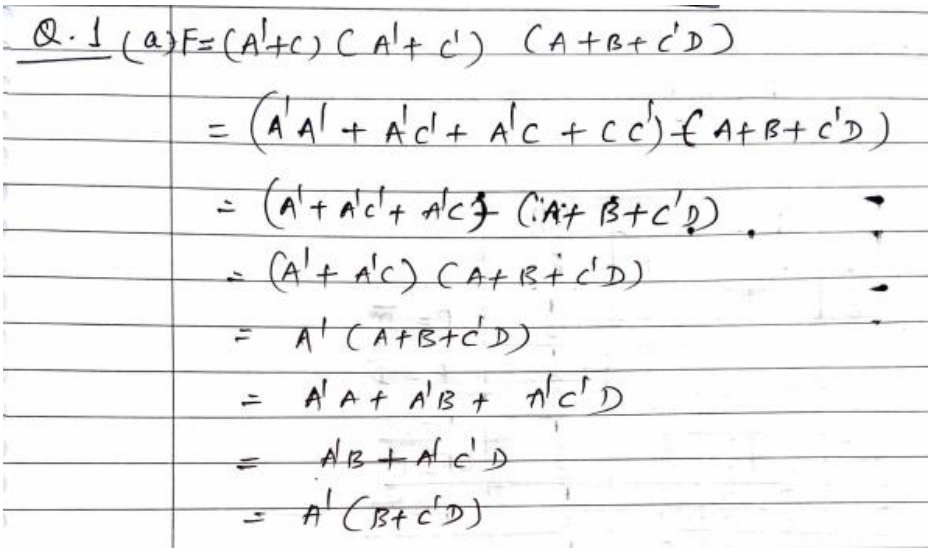
Course Name & code: Digital Systems Design (BECE102L)

Class Number (s): 3678, 3677, 3670, 3680, 4052

Faculty Name (s): (Dhanabal R, Tanmaya Kumar Das, Prayline Rajabai C, Nithish Kumar V, Shilpi Ruchi Kerketta)

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s): ANSWER ALL QUESTIONS

Q.No.	Question	Max Marks
1.	(a) Simplify the following Boolean expressions to a minimum number of literals using postulates. Also, determine the dual and complement of the simplified expression. $F = (A' + C)(A' + C')(A + B + C'D)$ (b) Realize the simplified expression of (a) using 2-input NAND gate only	10
		

Q.1 (a) $F = (A'+C)(A'+C')(A+B+C'D)$

$= (A'A' + A'C' + A'C + CC')(A+B+C'D)$

$= (A' + A'C' + A'C)(A+B+C'D)$

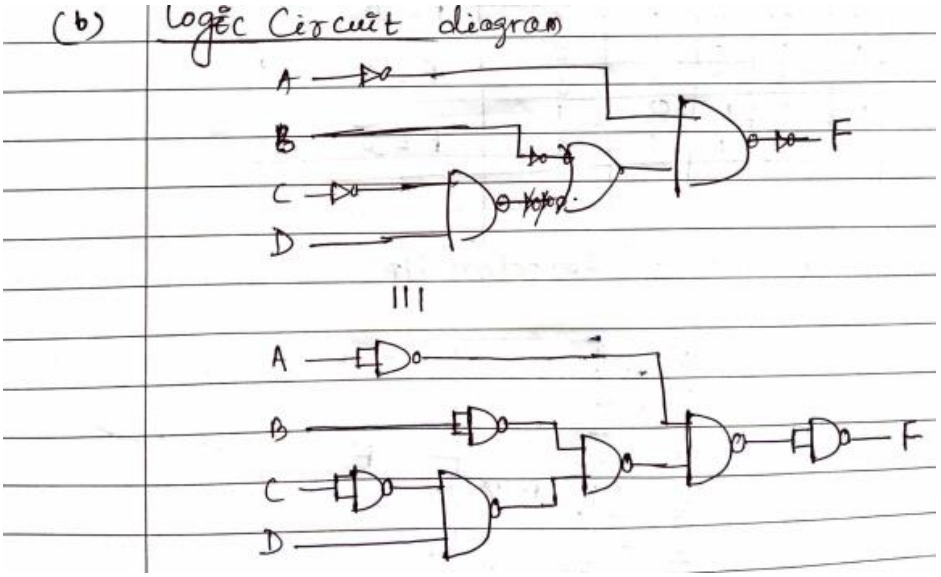
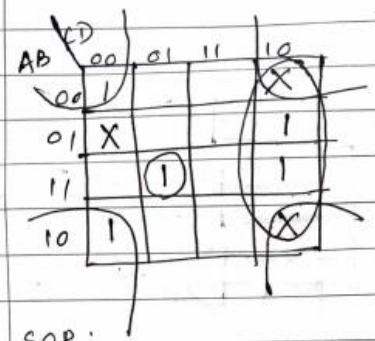
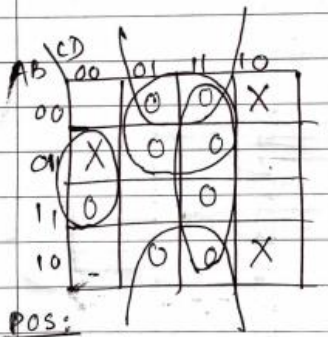
$= (A' + A'C)(A+B+C'D)$

$= A'(A+B+C'D)$

$= A'A + A'B + A'C'D$

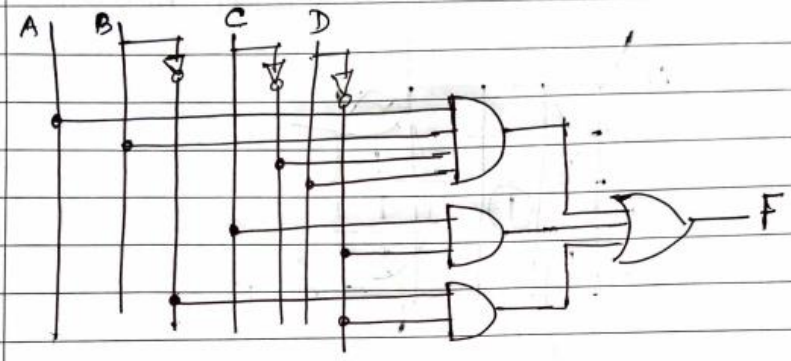
$= A'B + A'C'D$

$= A'(B + C'D)$

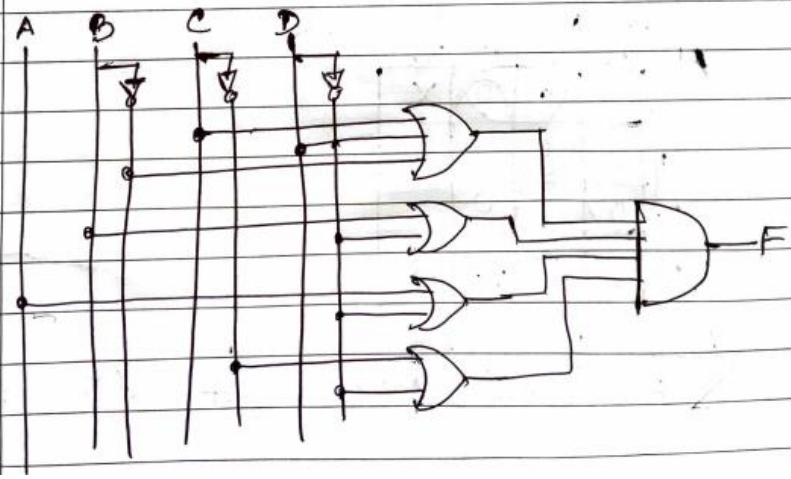
	(b) Logic Circuit diagram  	
2	Simplify the following Boolean function F, together with the don't-care conditions d, and then express the simplified function in sum-of-product form and product of sum. Draw the logical diagram of the function using minimum number of basic gates. $F\ (A, B, C, D) = \sum m(0, 6, 8, 13, 14) + d(2, 4, 10)$	10
	Q.8 $F(A,B,C,D) = \sum m(0,6,8,13,14) + \sum d(2,4,10)$  SOP: $F = C\cdot\bar{D} + \bar{B}\cdot\bar{D} + A\bar{B}\cdot\bar{C}\cdot D$  POS: $F = (\bar{C}+\bar{D})\cdot(A+\bar{D})\cdot(B+\bar{D})\cdot(\bar{B}+C+D)$	

Logical diagram

Using SOP: $F = C\bar{D} + \bar{B}\cdot\bar{D} + AB\bar{C}D$



Using POS: $F = (\bar{C}+\bar{D})\cdot(A+\bar{D})\cdot(B+\bar{D})\cdot(\bar{B}+C+\bar{D})$



3.	(a) Debug the errors in the following code.
	
	module 3_example (A, B, C, D, E, F) // Line 1 inputs A, B, C,
	Output D, E, F, // Line 2
	output D,E,F, // Line 3
	and g1(A, B, D); // Line 4
	not (E;A), // Line 5
	OR (F, B; C); // Line 6
	end module; // Line 7
		10

Q. 3(a)

```
module Example-3(A, B, C, D, E, F);
input A, B, C;
output D, E, F;
and g1(D, A, B);
not (E, A);
or (F, B, C);
endmodule
```

(b) Write the dataflow model for the design specified by thefollowing Verilog code.

```
module Circuit_A (A, B, C, D, F);input A, B,
C, D;
output F;
wire w, x, y, z, a, d;not (a, A);
not (d, D);
and (y, a , C);
or (x, B, C, d);
and (z, y, A);
and (w, z , B);
or (F, x, w);
endmodule
```

Q.3 (b)

```
module Circuit_A (A, B, C, D, F);
input A, B, C, D;
output F;
wire w, x, y, z, a, d;

assign a = ~A;
assign d = ~D;
assign y = a & C;
assign z = y & A;
assign w = z & B;
assign x = B | C | d;
assign F = x | w;
endmodule
```

(or)

```
module Circuit_A (A, B, C, D, F);
input A, B, C, D;
output F;

assign F = (B | C | (~D)) | (((~A) & C & A) & B);
endmodule
```

4.	A combinational circuit has three inputs, *x*, *y*, and *z*, and three outputs, *A*, *B*, and *C*. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the output is the two's complement of input. (a) Design the combinational circuit by finding the circuit'struth table, Boolean expression and the logic diagram. (b) Write the Verilog HDL code for the above circuit usinggate level model.	10

Q.4.(a) Combinational Circuit

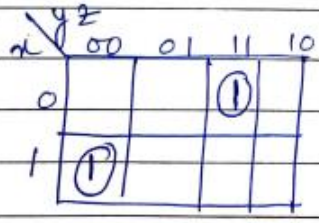
i/p: x, y, z

o/p: A, B, C

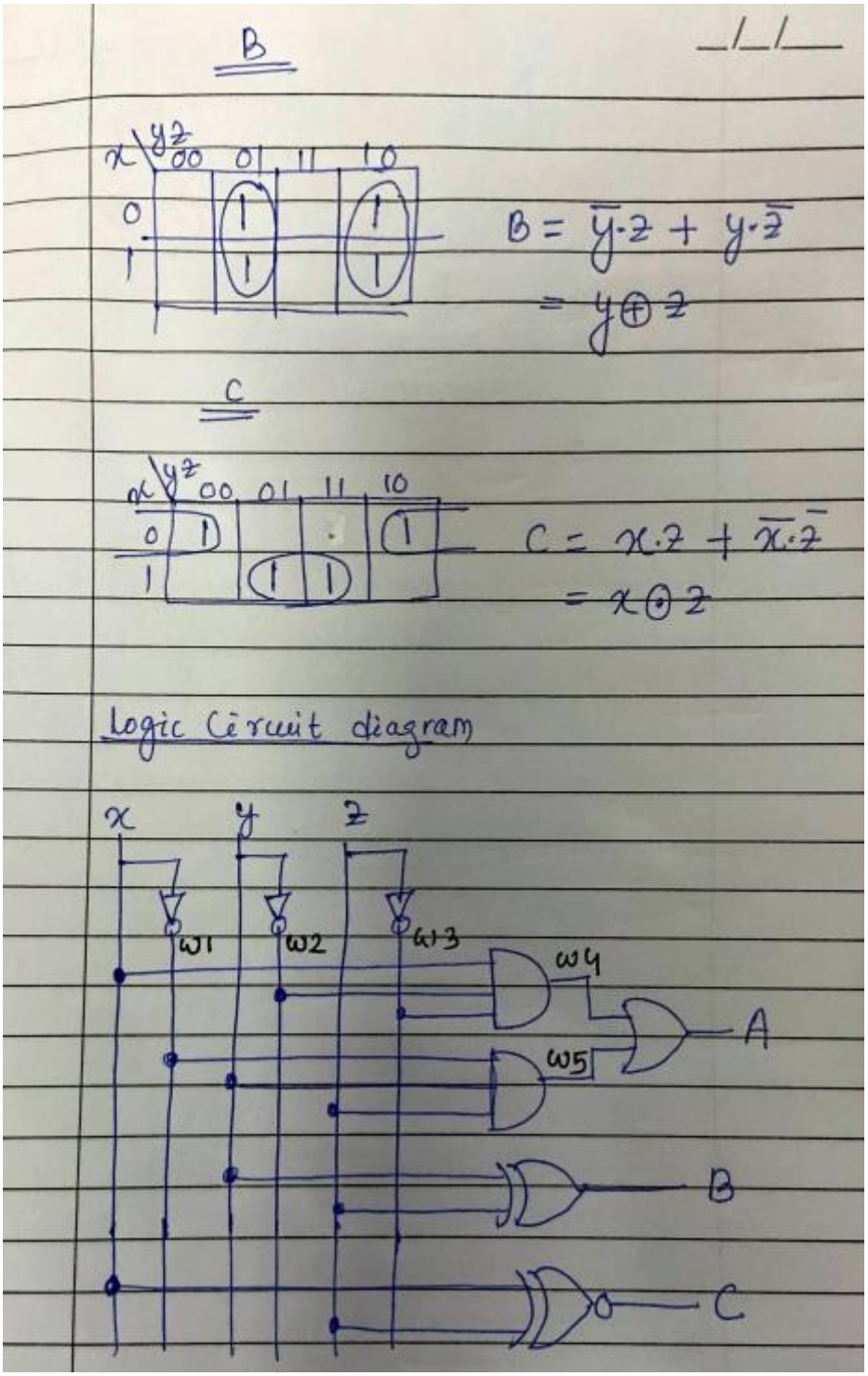
Truth Table

Input			Output		
x	y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	0	1

A



$A = x\bar{y}\bar{z} + \bar{x}yz$


B
_/_/_
x
yz
00
01
11
10
0
1
1
1
1
1
B = ȳ·z + y·z̄
= y ⊕ z
C
x
yz
00
01
11
10
0
1
1
1
1
1
C = x·z + x̄·z̄
= x ⊙ z
Logic Circuit diagram
x
y
z
w1
w2
w3
w4
w5
A
B
C

(b)

```
module Q4(x, y, z, A, B, C);

input x, y, z;
output A, B, C;
wire w1, w2, w3, w4, w5;

not g0(w1, x);
not g1(w2, y);
not g2(w3, z);

and g3(w4, x, w2, w3);
and g4(w5, w1, y, z);
or g5(A, w4, w5);

xor g6(B, y, z);
xnor g7(C, x, z);

endmodule
```

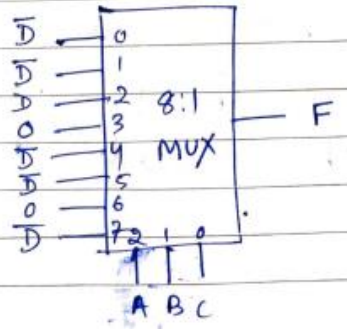
5.	Implement the Boolean function $F(A, B, C, D) = \sum m(0, 2, 5, 8, 10, 14)$ (a) using 8x1 multiplexer with A, B, C as select signals and (b) using 3 to 8 decoders with additional basic gates.	10

Q. 5

(a) $F(A, B, C, D) = \sum m(0, 2, 5, 8, 10, 14)$

I/P				O/P	
A	B	C	D	F	
0	0	0	0	1	$F = \overline{D}$
0	0	0	1	0	
0	0	1	0	1	$F = \overline{D}$
0	0	1	1	0	
0	1	0	0	0	$F = D$
0	1	0	1	1	
0	1	1	0	0	$F = 0$
0	1	1	1	0	
1	0	0	0	1	$F = \overline{D}$
1	0	0	1	0	
1	0	1	0	1	$F = \overline{D}$
1	0	1	1	0	
1	1	0	0	0	$F = 0$
1	1	0	1	0	
1	1	1	0	1	$F = \overline{D}$
1	1	1	1	0	

A, B, C → Selection i/p



Q.5

(b) $F(A, B, C, D) = \sum m(0, 2, 5, 8, 10, 14)$

3:8 decoder ⇒ 2 nos needed