C/L/TX

Reg. No:

VIT
Vellore Institute of Technology

# Final Assessment Test – November 2024

Course: BECE102L - Digital Systems Design
Class NBR(s): 3670 / 3677 / 3678 / 3680 / 4052
Time: Three Hours
Slot: D1+TD1
Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

**Answer ALL Questions**
**(10 X 10 = 100 Marks)**

1. i) Simplify the following Boolean expression using the Boolean algebraic theorems and postulates to a minimum number of literals.

   $F(w,x,y,z) = xy + x(wz + wz')'$

   ii) Represent the following boolean function in canonical SOP form.

   $F(A,B,C,D) = A + CD + (A + D')(C' + D)$

2. Simplify the following expressions to (i) standard sum-of-products and (ii) standard products-of-sums using K-Map and implement the simplified SOP function with two-level NAND gate circuit.

   $F = AC'D' + A'C + ABC + AB'C + A'C'D'$

3. Analyze the following statements with the inputs A = 4'b0011, B = 3'b011 and C = 3'b101 and compute the output Y. Represent in sized Number format.
   a) Y = A + (B | C)
   b) Y = 4'bx0x1 !== 4'bx0x1
   c) Y = (A || B) ? B : C
   d) Y = {4'bx0x1, 3{A}}
   e) Y = 1'bz <= 10

4. Many offices and buildings use combination locks to control the entry. As the design engineer of the Wonderful Door Security Company, you are asked to implement a door security system by using a card reader. There are four inputs to the card reader: inputs X, Y, and Z are used to validate the correct door code, and input V is used to check if the card reader is still valid. After the card reader is being read by the system, there are three outputs to this system: alarm (A), door open (D), and Error (E). Door (D) will only open when the decimal value of the binary inputs (X, Y, Z) is odd and the card reader is valid (V). The Error (E) signal goes on when the code on the card is correct (i.e. decimal value equal to odd) but the card is no longer valid. Finally, the alarm (A) will trigger when the code is incorrect. Show your final design with minimal logic gates.

5. Design a full subtractor circuit using 4x1 Multiplexers and additional gates. Write the structural modelling code in Verilog HDL for the full subtractor using 4x1 Multiplexers.

6. Design a magnitude comparator circuit to compare two 2-bit unsigned binary numbers. Using the 2-bit magnitude comparator circuit and additional logic gates, design a 4-bit magnitude comparator circuit. Write data flow level Verilog code.

7. A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.

(a) Tabulate the characteristic table.

(b) Derive the characteristic equation.

(c) Tabulate the excitation table.

(d) Show how the PN flip-flop can be converted to a T flip-flop.

8.(a) Design a sequential circuit using JK Flip-flop which transitions to the following states $0-1-3-5-7-0$.

(i) Draw the corresponding state diagram.

(ii) List the state table for the sequential circuit.

(iii) Design the circuit and draw the logic diagram of the circuit.

**OR**

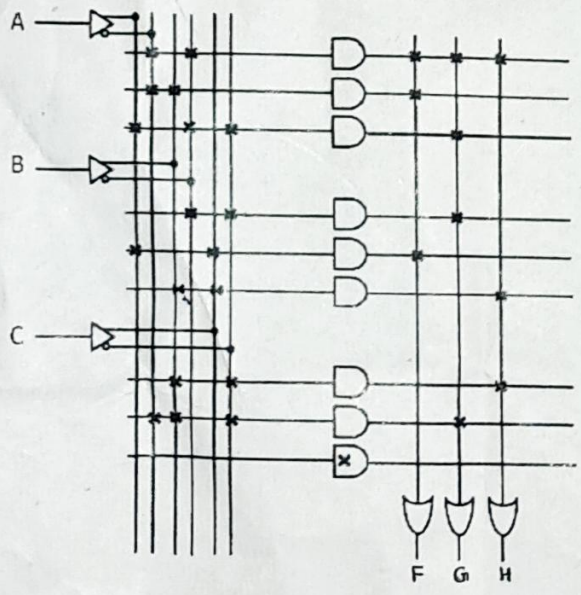
8.(b) Design the logic diagram of a 4-bit shift register with mode selection inputs S0 and S1. The register is operated according to the following: S0=S1=0: hold the current state, S0=1 and S1=0: Shift left, S0=0 and S1=1 : load parallel input data, S0=S1=1 : clear register to 0.

9.(a) Draw a state diagram and write a behavioural Verilog code of a Mealy synchronous state machine having a single input, x_in, and a single output y_out, such that y_out is asserted if the total number of 1's received is a multiple of 3.

**OR**

9.(b) Design a Moore FSM using T-FFs which has a single input, x_in, and a single output y_out, such that y_out is asserted if the total number of 0's received is a multiple of 3. Write a behavioural Verilog code.

10. Implement the PLA circuit given below using PROM.

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