Final Assessment Test – November 2024

VIT
Vellore Institute of Technology

Course: BEVD204L - Electronic Circuits
Class NBR(s): 4065
Time: Three Hours

Slot: A1+TA1
Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

Answer ALL Questions
(10 X 10 = 100 Marks)

1. a) Derive the stability factor of Common Emitter BJT configuration. Define stability factor.

   b) What is mean by Operating point? Derive the expression for the I_B, I_C and V_{CE} of the voltage divider biasing BJT circuit.

2.(a) i) Determine the voltages at all nodes and the currents in all branches. The minimum value of β is specified to be 30.

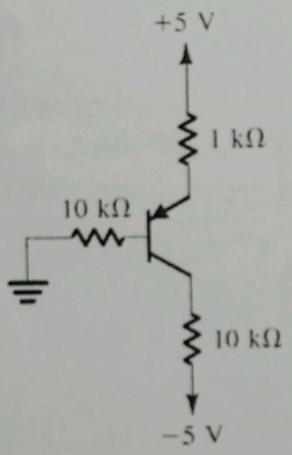

Fig. 1

ii) In the circuit shown in Fig. 2, the voltage at the emitter was measured and found to be –0.7 V. If β = 50, find I_E, I_B, I_C, and V_C.

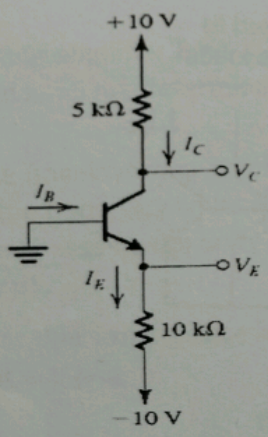

Fig. 2

OR

2.(b) Determine the resistor values to meet this specification given below for the circuit shown in Fig.3. V_{cc} = 10 V, I_c = 9 mA, V_{CE} @ midpoint and β = 100.

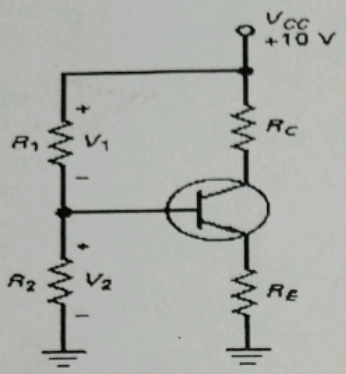

Fig. 3

3. Determine the small-signal voltage gain and input resistance of a common-emitter circuit with an emitter resistor. For the circuit in Fig. 4, the transistor parameters are β = 100, V_{BE} (on) = 0.7 V, V_A =∞. I_{CQ} = 2.16 mA. V_{CEQ} = 4.81 V.

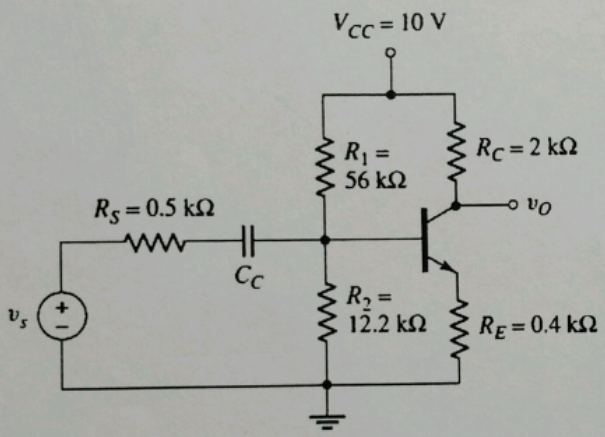

Fig. 4

4. a) All the transistors used in the circuit given in Fig. 5 are matched and have a current gain β of 20. Calculate the current I_{O4}? Neglect the early effect.

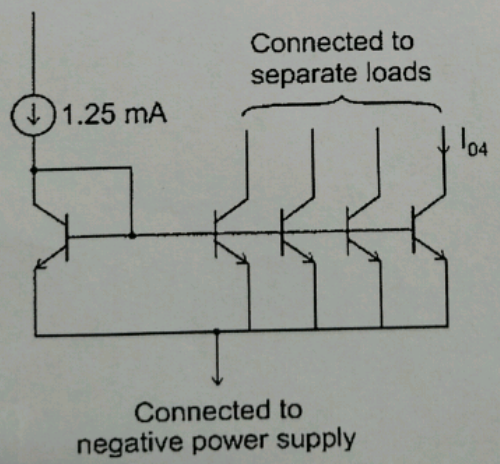

Fig. 5

b) Find the output impedance and gain of given circuit in Fig. 6

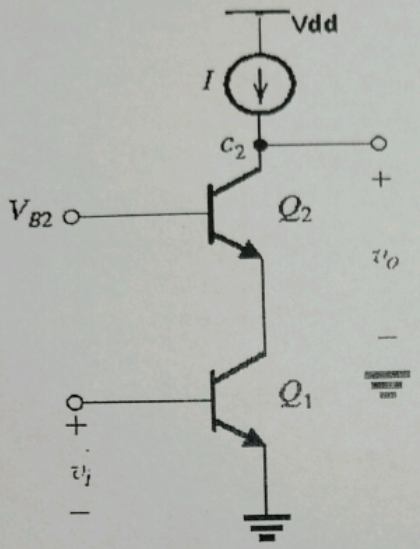

Fig. 6

5. The circuit shown in Fig. 7 has the following parameters R_C= 4 KΩ, R'= 40 KΩ, R_S= 10 KΩ, h_{ie} = 1.1 KΩ, h_{fe}=50, h_{re}=h_{oe}=0. Identify the topology and find the A_{vf}, R_{if} and R_{of} for the feedback network.

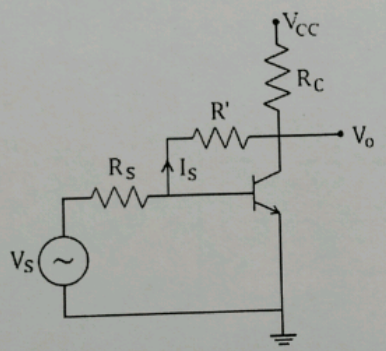

Fig. 7

6. a) For an inverting amplifier R_1=1 kΩ, R_f=10 kΩ. If the op-amp has V_{ios}=20 mV, I_B= 60 nA and I_{ios}=5 nA, determine the maximum output offset voltage due to V_{ios}, I_B, I_{ios}.

b) Consider the non–inverting amplifier circuit with R_f = 24 kΩ and R_1 = 1 kΩ. Investigate the frequency limits of operation when the input signal has a peak value of 20 mV, assume the unity gain bandwidth (UGB) to be 1 MHz and Slew rate = $0.5V/\mu S$.

7.(a) Design an circuit that can produce an output V_O= -(3V_1+2V_2+4V_3), where V_1, V_2, V_3 are the input voltages. **BL3 CO3**

OR

7.(b) Design a voltage series feedback amplifier, R_1 = 470 Ω and R_f = 4.7 kΩ. Assume that op-amp is a 741 having the following specifications. A = 200000, Ri = 2 M Ω, Ro = 75 Ω, fo = 5 Hz, Vcc = +/- 15 V. Calculate and compare the values of with and without feedback gain, bandwidth, input impedance.

8. A positive peak detector is used along with a simple comparator in Fig. 8 to monitor input levels and warn of possible overload. The LF412 is a dual-package version of the LF411. Explain how it works and determine the point at which the LED lights. Plot the input and output of peak detector and justify your assumption when LED glows.

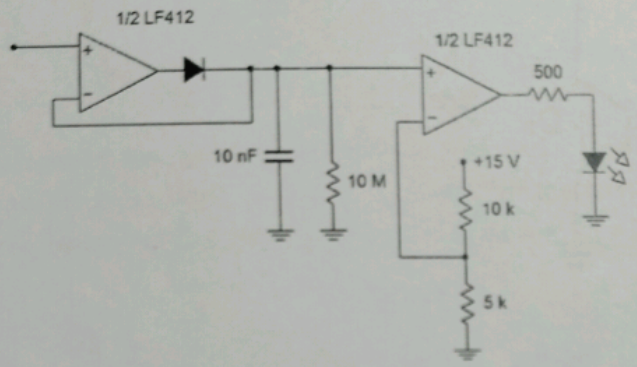

Fig. 8

9. Design and implement a Schmitt trigger circuit whose upper threshold voltage (V_{UT})= 1.36 V and lower threshold voltage (V_{LT})= -1.09 V.

10. Calculate the values of resistors and capacitors shown in Fig. 9 to sustain its oscillations at f_o = 25 kHz. The minimum resistance used is to be 10 kΩ. Derive the expression for f_o.

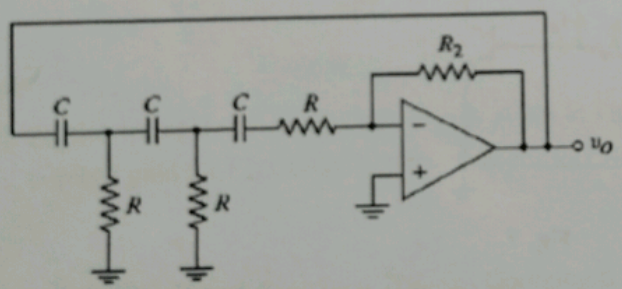

Fig. 9

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