J/E/TX

Reg. No:

Final Assessment Test – May 2024

VIT®
Vellore Institute of Technology

Course: BCSE205L - Computer Architecture and Organization

Class NBR(s):0775/0782/0790/0799/0804/0806/ 0824/0826/0843/0851/0856/0867/0873/0880/0888/ 0889/0893/0895/0897/0899/0903/0908/0915 Slot: **D1+TD1**

Time: Three Hours Max. Marks: **100**

- KEEPING MOBILE PHONE/ELECTRONIC DEVICES EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

Answer any TEN Questions

(10 X 10 = 100 Marks)

1. a) Write an assembly language code for the following expression using the IAS computer Instruction set. [6]

   A = (B+C) * D. Assume that the inputs are available in the memory location 450, 451 and 452. Store the results in memory location 750 and 751.

   b) Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder of the immediate operand or an operand address. Discuss the impact on the system speed if the microprocessor bus has a 32-bit local address bus and a 16-bit local data bus. How many bits are needed for the program counter and the instruction register? [4]

2. a) Having multiplicand as 13 and multiplier as (-7), find the product using Booth's algorithm with appropriate flow diagram and step by step description. [7]

   b) Represent 1250.125_{10} as floating-point number in single precision format. [3]

3. a) Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs: [6]

Instruction Type	Instruction Count (millions)	Cycles per instructions
Machine A	8	1
	4	3
	2	4
	4	3
Machine B	10	1
	8	2
	2	4
	4	3

Determine the effective CPI, MIPS rate, and execution time for each machine. Comment on the results.

b) Enumerate and explain the procedure in the phases of Instruction cycle with a state diagram. [4]

4. a) A two-way set-associative cache has lines of 16 bytes and a total size of 8 Kbytes. The 64-Mbyte main memory is byte addressable. Show the format of main memory addresses. [6]

b) Discuss the memory hierarchy in terms of size, access time and cost per bit. [4]

5. In cache memory management policies, explain the process of the page replacement algorithm FIFO with the cache lines of 4 frames and 6 frames. Show each step in detail and comment on the hit ratio and miss ratio obtained for both the frames.

1 2 3 4 2 1 5 6 2 1 2 3 7 6 2 3 7 2 3 6

6. How many 1024x8 RAM chips are needed to provide a memory capacity of 2048x8? Draw the address map table and the chip organization with memory connection to CPU.

7. a) A computer system needs to transfer a large block of data from RAM to an external device such as hard drive. Explain how DMA can improve data transfer in this scenario. Also show the DMA configurations with relevant diagrams. [7]

b) DMA controller has a transfer rate of 10 MB/s. If it takes 100 milliseconds to transfer a block of data, what is the size of the block? [3]

8. With a flow diagram, explain the interrupt driven Input Output Module. Discuss the different interrupt handling mechanisms and brief out the Interrupt overhead.

9. a) Discuss the salient features of the Magnetic Disk with its structural representation. List out the pros and cons of the magnetic disk. [6]

b) Assuming an even parity, detect and correct the errors in the 7-bit hamming code 1011011. [4]

10. a) Differentiate block striping and mirroring Redundant Array of Independent Disk. [4]

b) A company's IT department wants to ensure data integrity and fault tolerance for its critical data storage. They have a large number of disks available for the array. Which RAID level would be the most appropriate choice, and what factors would you consider in making your recommendation? [6]

11. Classify Flynn's taxonomy of parallel computer architecture with suitable examples of each.

12. a) In a pipelined processor, a sequence of instructions is being executed. The third instruction requires the result of the first instruction as an operand. However, the result of the first instruction is not yet available when the third instruction needs it. Identify the type of hazard occurring in this scenario and propose a solution to mitigate it. [5]

b) Compare and contrast superscalar versus super pipeline architecture. [5]

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