F/E/TX

Reg. No:

VIT®
Vellore Institute of Technology

Final Assessment Test – May 2024

Course: **BECE303L - VLSI System Design**

Class NBR(s): **3816** Slot: **A1+TA1**

Time: **Three Hours** Max. Marks: **100**

- **KEEPING MOBILE PHONE/ELECTRONIC DEVICES EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE**
- **DON'T WRITE ANYTHING ON THE QUESTION PAPER**

Answer any TEN Questions

(10 X 10 = 100 Marks)

1. A MOSFET is constructed using 65nm CMOS technology on N type of substrate, by diffusing Indium impurities for source and drain regions.

   NMOS: K_n=115μA/V^2, V_{T0} =0.43V, λ =0.06 V^{-1} W/L=10

   PMOS: K_p=30μA/V^2, V_{T0} =-0.4V, λ =-0.1 V^{-1} W/L=10

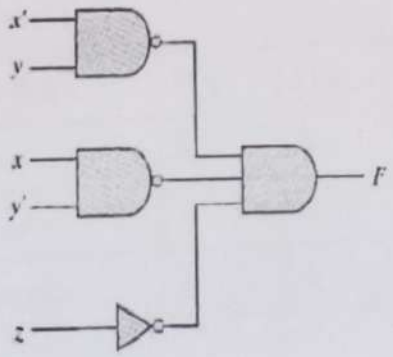
   a) Identify the operating region of the above MOSFET, when the following voltages are applied for the gate, source and drain terminals

   b) Calculate the drain current in each case.

S.No	V_G (V)	Vs(v)	V_D (V)
1	0	2.0	0.2
2	0	2.0	1.3
3	0	2.0	0

2. Explain the following non ideal effects
   (a) Channel Length Modulation
   (b) Velocity Saturation
   (c) Mobility Degradation
   (d) Body Effect
   (e) Subthreshold Conduction

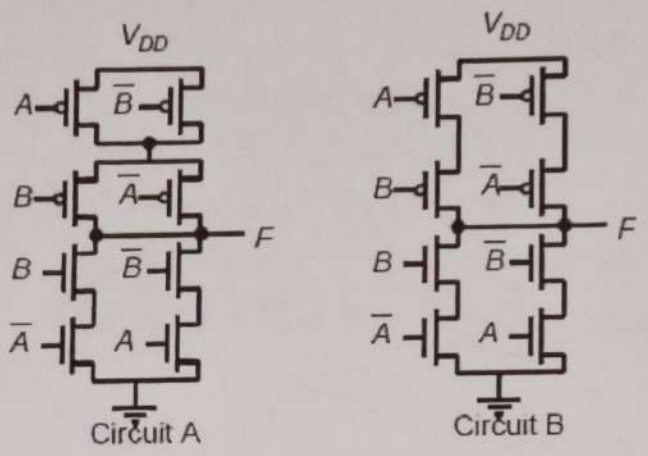
3. The following figure shows a simple logic function realized with three variables. Find out the expression for F and develop a CMOS logic circuit for it.



Mention the width of each gate in the implemented circuit in terms of *w*, if it has to be as faster as the unit sized inverter. The resistance of PMOSFET in the unit inverter is 2.5 times that of NMOSFET.

4. Implement transmission gate logic based T-Flip Flop and explain its operation with neat timing diagrams.

5. i) What is the logic function of circuit A and circuit B in the figure shown below? Will these two circuits rise and fall times always be equal to each other? Why or why not?

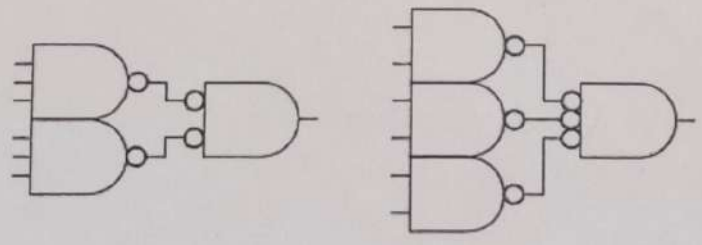


ii) Find out their rise time if all NMOSFETs in the above circuit have a size of 2w and PMOSFETS have a size of 4w.

6. Design a CMOS logic for the function $F = \overline{AB + C}$, with transistor widths chosen to achieve effective rise and fall resistance equal to that of a unit inverter. Calculate the worst case fall and rise delay.

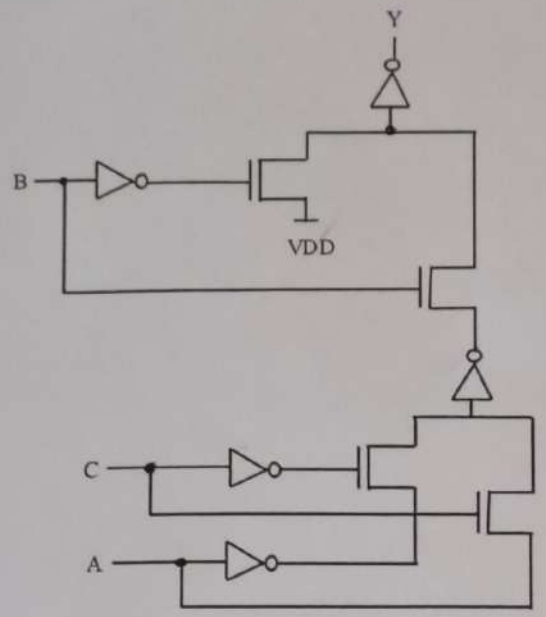
7. Design the function $F = \overline{A + B + CD + E}$ in static CMOS logic using least number of transistors. Draw the stick diagram and estimate the area.

8. Consider two designs ((a) and (b)) of a 6-input AND gate shown in Figure below. Develop an expression for the delay of each path if the path electrical effort is H. What design is fastest for H = 1? For H = 5? For H = 20? Explain your conclusions intuitively.



(a) (b)

9. Consider the pass transistor logic given in the figure below. Derive the output expression for Y and write the truth table for the corresponding logic function.

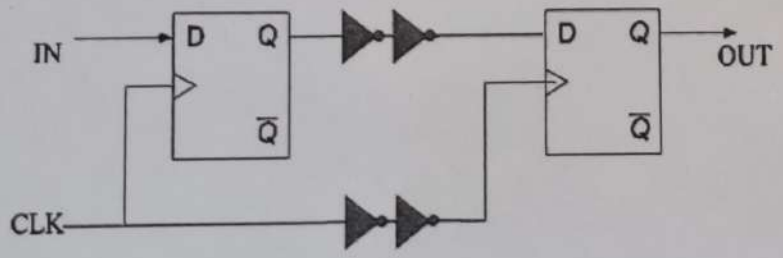


10. Sketch a pseudo-nMOS gate that implements the function F.

$$F = \overline{AB + CD + EF + G}$$

Size the pseudo-NMOS with PMOS transistors 1/4 the strength of the pulldown stack. Also calculate logical effort Note: Assume for equal drive strength, PMOS width and NMOS width ratio, (Wp: Wn) is 2:1.

11. Consider the below flip flop pair logic diagram and the table with three different flip flops FF1, FF2, and FF3 with their timing specifications.



Which combination of flip flops should be replaced in the below flip flop pair to get the maximum clock frequency of operation. (Assume The inverters have a delay of 1ns each)

Flip-flops	FF1	FF2	FF3
T_{CLK-Q}	5	6	8
$T_{setup\ time}$	3	4	2
T_{hold_time}	2	1	1

12. Draw the circuit diagram of 6-T SRAM cell and also explain in detail the Read and Write operation of 6-T SRAM cell.

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