VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

School of Electronics Engineering (SENSE)

Fall Semester 2024-25

Continuous Assessment Test - I

SLOT: G1+TG1

Programme Name & Branch: B. Tech & CSE (BCB, BCE, BCI, BCT, BDS, BKT)

Course Name & Code: Microprocessor & Microcontrollers (BECE204L)

Class Number (s):VL2024250104321, VL2024250104315, VL2024250104323, VL2024250104343, VL2024250104331, VL2024250104318, VL2024250104334, VL2024250104328, VL2024250104326

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Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

Specify if any printed material may be permitted

Any other specific instruction

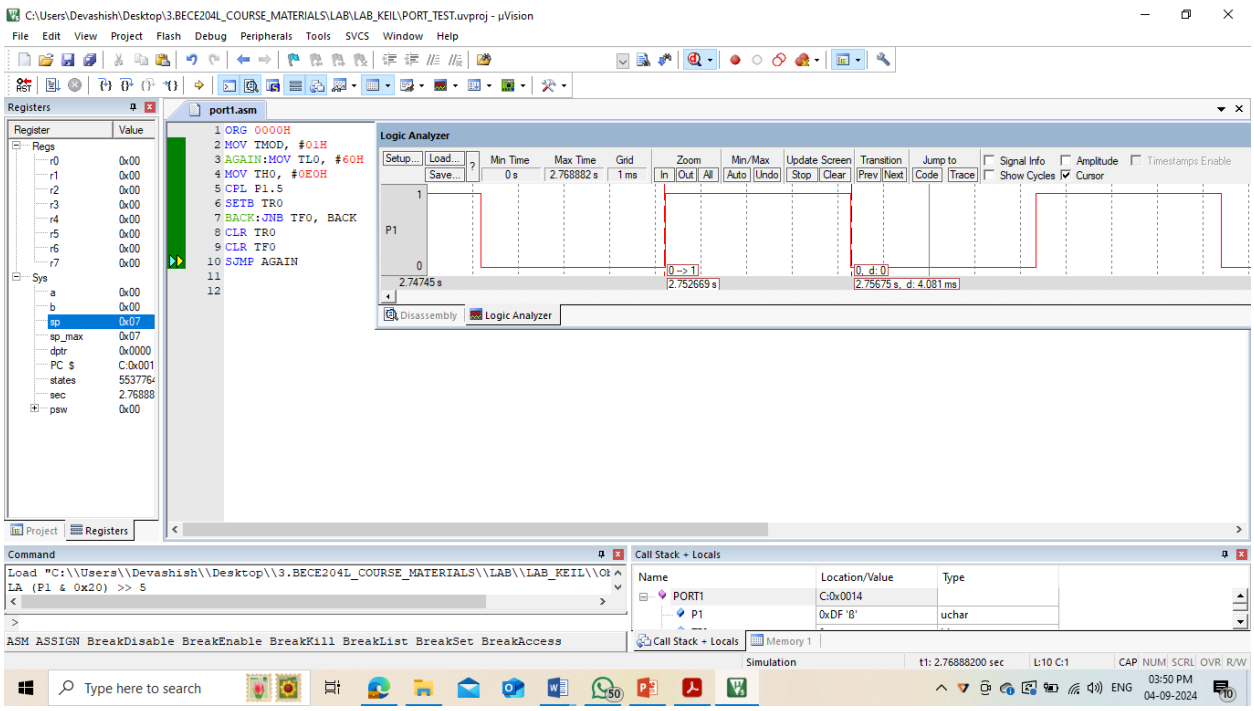
Q. No.	Question	Max Marks
1.	Write an 8051 based program assuming the crystal frequency is 12MHz, find the timer register values if we want to have a time delay of 8ms? Also generate the 8ms pulse width with equal amount of ON and OFF period using timer 0 and through 16-bit mode of operation.	10
2.	Write an 8051 assembly program to read port 0. If received data is equal to AAH, send the data "BBH" to port 1, else send the data "CCH" to port 2.	10
3.	**a)** Show the status of PSW register in 8051 after the subtraction performed between 93H and 88H. **b)** In a version of 8051, the crystal frequency is 13.0592MHz. Find the time delay associated with **loop** section of the following DELAY subroutine. DELAY: MOV R5, #200 HERE: NOP NOP NOP NOP DJNZ R5, HERE RET	5+5
4.	Compare microprocessor with microcontroller with neat block diagram, explaining the blocks in detail.	10
5.	Write an 8051 assembly language program to add the odd numbers stored in code memory from the location 300H to 309H. The stored data's are: 84H, 22H, 33H, AAH, CCH, 48H, 21H, 12H, 76H and 67H. Store the summation of odd numbers at location 62H and 63H of RAM.	10

ANSWER KEY FOR G1+TG1 (CAT-1)

1. Given crystal frequency is 12MHz. So for one machine cycle execution, system will take 1uS.

The desired time delay given is 8milli second. ON and OFF time is equal. So it's a square wave. So 8mS/1uS= 8000 clock pulses for ON and OFF period.
65536 – 8000 = 61536 = 0F060H.

TH0 = 0E0H
TL0 = 60H



2.

```
ORG 0000H
MOV P0, #0FFH
MOV A, P0
CLR C
SUBB A, #0AAH
JZ LOOP1
MOV A, #0CCH
MOV P3, A
SJMP LOOP2

LOOP1: MOV A, #0BBH
       MOV P2, A
LOOP2: NOP
END
```

3. A. 93H – 88H =
93H = 1001 0011
88H = 1000 1000

After subtraction 0000 1011 which is 11 in decimal. 93H is equivalent to 147D and 88H equivalent to 136D.

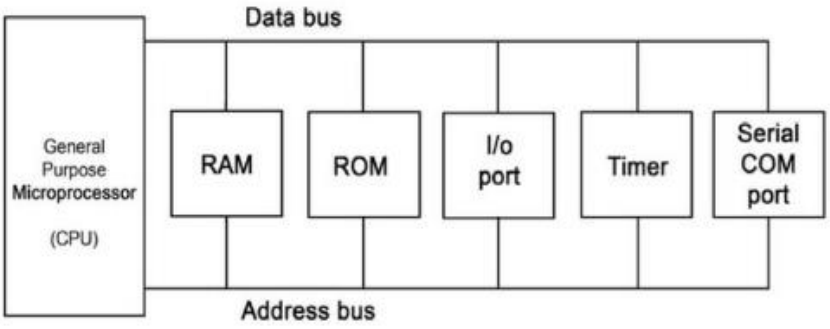
AC = 1
Cy = 0
P = 1
Ov = 0

PSW = 0 1 0 0 0 0 0 1 = 41H

B. For the frequency, 13.0592MHz, the machine cycle execution time can be found as 0.9uS.

The time delay inside HERE loop is [200(1+1+1+1+2)*0.9uS] = 1080uS
Adding the two instructions outside the loop we have 1080uS+3*0.9uS = 1082.7uS.

4.



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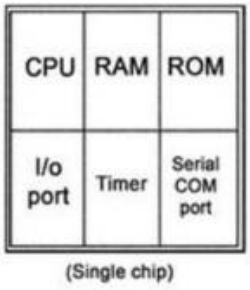

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