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School of Computer Science Engineering

Fall Semester 2024-2025

Continuous Assessment Test – I

Program Name & Branch: BTECH CSE (BCB, BCE, BCI, BCT, BDS, BKT)

Course Name & code: BECE204L Microprocessors and Microcontrollers

Slot: G2+TG2

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

Answer all the questions

<table>
<tr><th>S. No</th><th>Question</th><th>Marks</th><th>CO</th><th>BL</th></tr>
<tr><td>1. A</td><td>Draw the generalised architecture microcontroller and explain</td><td>5</td><td>1</td><td>1</td></tr>
<tr><td>1. B</td><td>Write the functions of following registers and buses
(i) Program counter
(ii) Stack Pointer
(iii) Data bus
(iv) Address bus
(v) Control bus</td><td>5</td><td>1</td><td>1</td></tr>
<tr><td>2</td><td>Analyze the following 8051 assembly program which consist 16 lines and Comment for each lines

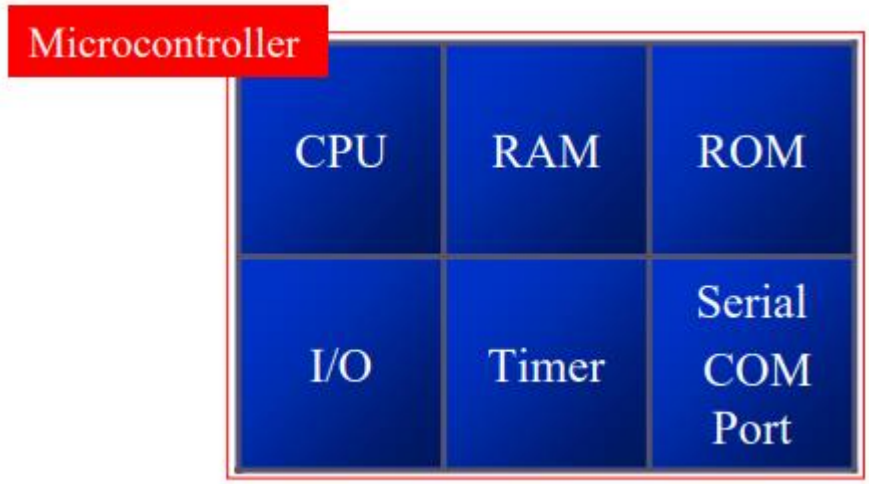
<table><tr><th>Line No</th><th>Instruction</th><th>Line No</th><th>Instruction</th></tr><tr><td>1</td><td>MOV R7, #25H</td><td>9</td><td>ADD A,B</td></tr><tr><td>2</td><td>SETB RS1</td><td>10</td><td>PUSH 07H</td></tr><tr><td>3</td><td>CLR RS0</td><td>11</td><td>PUSH 0FH</td></tr><tr><td>4</td><td>MOV R7,#12H</td><td>12</td><td>PUSH 17H</td></tr><tr><td>5</td><td>MOV A,#00H</td><td>13</td><td>POP 0DH</td></tr><tr><td>6</td><td>ADD A, R7</td><td>14</td><td>POP 0CH</td></tr><tr><td>7</td><td>MOV 0FH,#0DEH</td><td>15</td><td>POP 0BH</td></tr><tr><td>8</td><td>MOV B,0FH</td><td>16</td><td>END</td></tr></table></td><td>10</td><td>3</td><td>2</td></tr>
<tr><td>3</td><td>Write an ALP to store the string “ALL IS WELL” from ROM addresses 250H to 25AH. Copy the string and store it in reverse order from RAM address 50H to 5AH.</td><td>10</td><td>3</td><td>3</td></tr>
<tr><td>4</td><td>Assume a switch is connected at port pin P0.2, monitor the status of the switch. If the status of the switch is HIGH (“1”) then transfer data from Port P1 to P3, else transfer data from P1 to R7 of Bank2.</td><td>10</td><td>4</td><td>3</td></tr>
</table>

5	Write an 8051 assembly program to generate a signal at p1.5 with 4ms on time and 8ms off time. Assume clock frequency of 8051 is 12 MHz and use the mode1 timer T0.	10	4	3

1. A. Draw the generalised architecture block diagram of microcontroller and explain briefly about all blocks:

Ans:

Block diagram (2 Marks)



Explanation (3 Marks)

1. B. Write the functions of following registers and buses

Ans:

(i) Program counter: It holds address of next instruction

(ii) Stack Pointer: It keeps top of the data of the stack.

(iii) Data bus: It carries the data.

(iv) Address bus: It carries address location.

(v) Control bus: It carry the control word to control the operation/program.

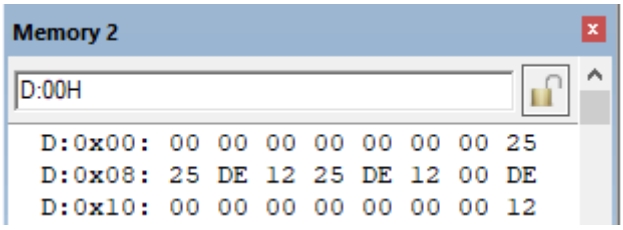
2. Analyze the following 8051 assembly program and show the output values each of the register and RAM memory location with neat sketch:

Line No	Instruction	Bank	Register	RAM Location	Stack Pointer
1	MOV R7, #25H	0	R7 ← #25h	07H	07H
2	SETB RS1	-	-	-	
3	CLR RS0	-	-	-	
4	MOV R7,#12H	2	R7 ← #12h	17H	07H
5	MOV A,#00H	-	A ← #00h	-	-
6	ADD A, R7	Bank 2, R7	A ← #12H	-	-
7	MOV 0FH,#0DEH	Bank 1	-	0FH ← #0DEH	-
8	MOV B,0FH	-	B ← #0DEH	-	-
9	ADD A,B	-	A ← #0F0H	-	-
10	PUSH 07H	0	R7	08H	SP = 08H ← #25H
11	PUSH 0FH	1	R7	09H	SP = 09H ← #0DEH
12	PUSH 17H	2	R7	0AH	SP = 0AH ← #12H
13	POP 0DH			0DH ← #12H	SP = 09H ← #0DEH
14	POP 0CH			0CH ← #0DEH	SP = 08H ← #25H
15	POP 0BH			0BH ← #25H	SP = 07H
16	END				

A = 0F0H, B = 0DEH, SP = 07H, 07H = 25H, 0FH = 0DEH, 17H = 12H, 08H = 25H, 09H = 0DEH, 0AH = 12H, 0BH = 25H, 0CH = 0DEH, 0DH = 12H

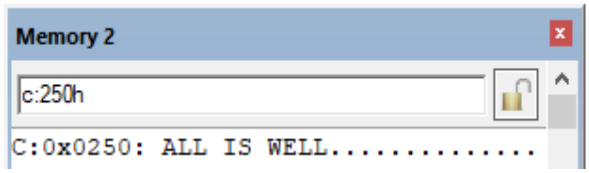
```
 1 MOV R7, #25H
 2 SETB RS1
 3 CLR RS0
 4 MOV R7,#12H
 5 MOV A,#00H
 6 ADD A, R7
 7 MOV 0FH,#0DEH
 8 MOV B,0FH
 9 ADD A,B
10 PUSH 07H
11 PUSH 0FH
12 PUSH 17H
13 POP 0DH
14 POP 0CH
15 POP 0BH
16 END
```

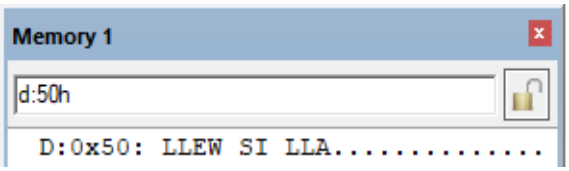
a 0xf0
b 0xde
sp 0x07



3. Write an ALP to store the string "ALL IS WELL" from ROM addresses 250H to 25AH. Copy the string and store it in reverse order from RAM address 50H to 5AH.

```
ORG  0250H
DB "ALL IS WELL"
ORG 0000H
MOV DPTR,#0250H
MOV R1,#5AH
MOV R7,#11
LOOP: CLR A
MOVC A,@A+DPTR
MOV @R1, A
INC DPTR
DEC R1
DJNZ R7, LOOP
HERE: SJMP HERE
END
```

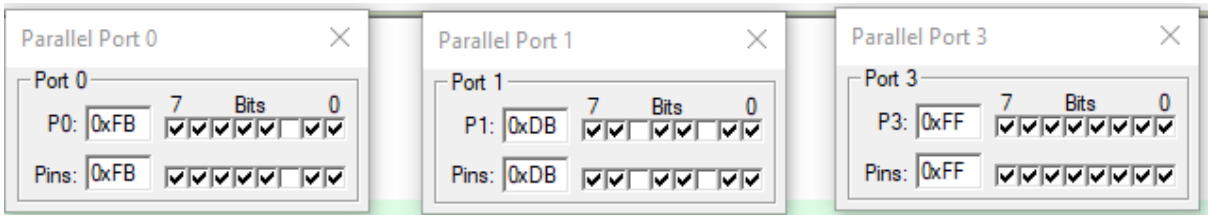


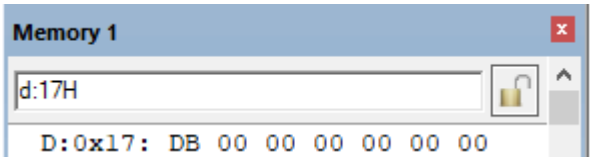


4. Assume a switch is connected at port pin P0.2, monitor the status of the switch. If the status of the switch is HIGH ("1") then transfer data from Port P1 to P3, else transfer data from P1 to R7 of Bank2.

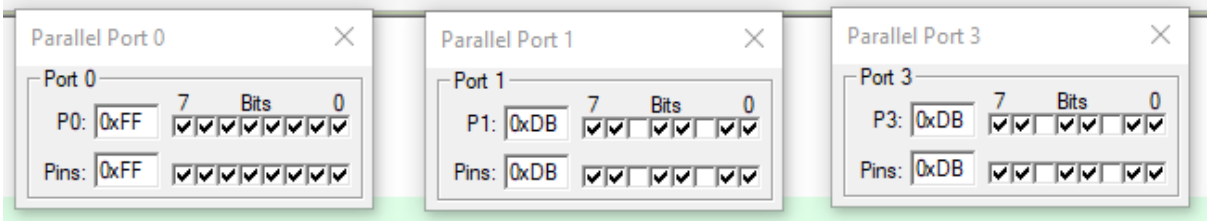
```
BEGIN:JB P0.2, TRUE
MOV 17H,P1
SJMP BEGIN
TRUE: MOV P3,P1
SJMP BEGIN
END
```

P0.2 = 0, P1 = 0DBH, (RAM LOCATION) 17H = 0DBH, P3 = 0FFH (DEFAULT VALUE)





P0.2 = 0, P1 = 0DBH, P3 = 0DBH (DEFAULT VALUE)



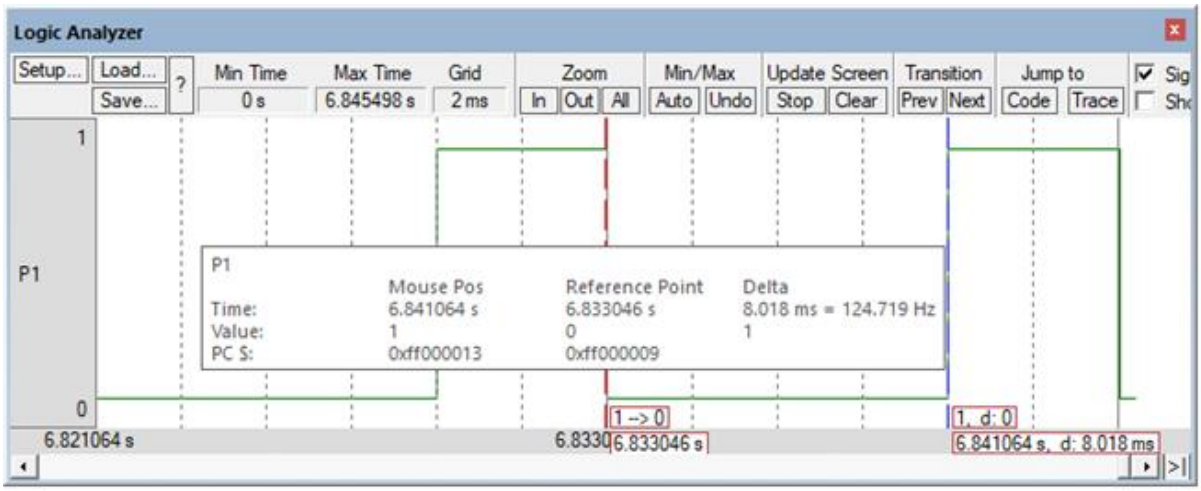
5. Write an 8051 assembly program to generate a signal at p1.5 with 4ms on time and 8ms off time. Assume clock frequency of 8051 is 12 MHz and use the mode1 timer T0.

Ans:

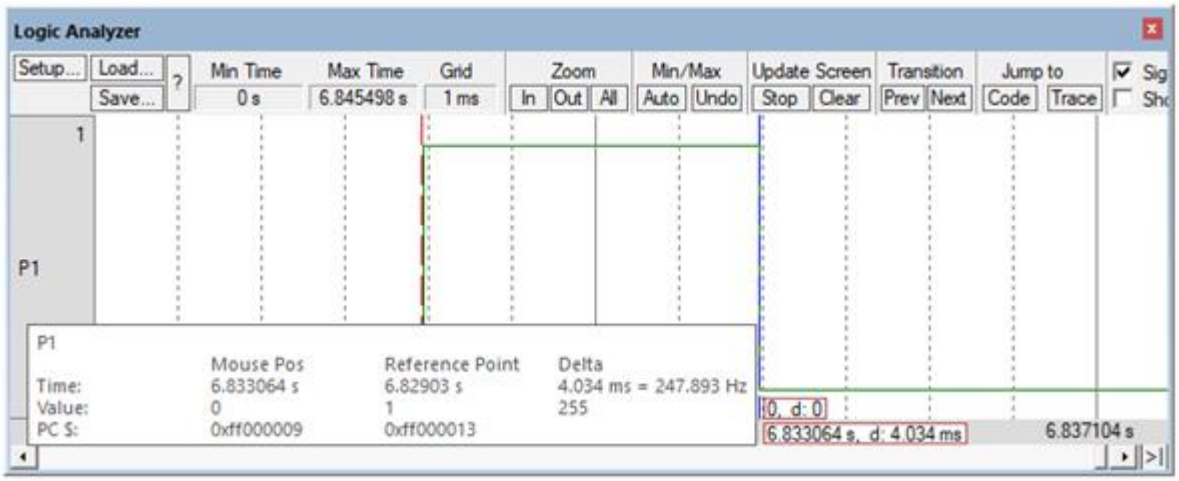
f_c = 12 MHz, T_c = 1/12 M Hz, 1 Machine cycle time = 1 µs.
Required ON time = 4 ms = 4000 µs, Required OFF time = 8000 µs.
Load value for ON time is = 65536 - 4000 = 61536 = 0F060H
Load value for OFF time is = 65536 - 8000 = 57536 = 0E0C0H

```
ORG 0000H
 MOV TMOD,#01H
 HERE: MOV TL0,#0C0H
 MOV TH0,#0E0H
 CPL P1.5
 ACALL DELAY
 MOV TL0,#60H
 MOV TH0,#0F0H
 CPL P1.5
 ACALL DELAY
SJMP HERE
 DELAY: SETB TR0
 AGAIN: JNB TF0, AGAIN
 CLR TR0
 CLR TF0
 RET
 END
```

OFF Time: 8 ms



ON Time: 4 ms


Logic Analyzer
Setup...
Load...
Save...
?
Min Time
0 s
Max Time
6.845498 s
Grid
1 ms
Zoom
In
Out
All
Min/Max
Auto
Undo
Update Screen
Stop
Clear
Transition
Prev
Next
Jump to
Code
Trace
Sig
Sho
1
P1
P1
Mouse Pos
Reference Point
Delta
Time:
6.833064 s
6.82903 s
4.034 ms = 247.893 Hz
Value:
0
1
255
PC $:
0xff000009
0xff000013
0, d: 0
6.833064 s, d: 4.034 ms
6.837104 s