

**VIT**

Vellore Institute of Technology

School of Computer Science Engineering and Information Systems

Fall Semester 2024-25

Continuous Assessment Test – 1

SLOT A2+TA2

Programme Name & Branch : B.Tech. IT

Course Name & code: Operating Systems & BITE303L

Class Number (s): VL2024250103319, VL2024250103339, VL2024250103349

Faculty Name (s): Dr. P J Kumar, Dr.M.Priya, Dr.S.MEENATCHI

Exam Duration: 90 Min.

Maximum Marks: 50

Answer All Questions (5*10=50)

Q.No.	Question	Max Marks																								
1.	Determine the role of the following in a computing system and briefly discuss the responsibilities of each. i) Boot Strap Loader ii) Buses iii) Cache Memory iv) Device drivers and Device Controllers v) Kernel	10																								
2.	Identify and discuss in brief various responsibilities of an operating systems.	10																								
3.	Illustrate with a program or pseudocode the steps involved in creating a child process with suitable functions using POSIX API. Also illustrate the process of assigning a new task to the child. How to synchronize parent and child process?	10																								
4.	Analyze the restrictions imposed on processes while accessing the memory. Identify and briefly discuss various approaches available for Inter Process Communication with a neat sketch.	10																								
5.	Apply Priority (Preemptive) and SJF (Non Preemptive) scheduling to the below scenario and draw Gantt chart to illustrate process execution. Assume that, smaller number represents higher priority. Calculate average waiting time and average turnaround time for each of the scheduling algorithm. Identify the scheduling algorithm that provides the least Average waiting time and turnaround time. <table><tr><th>Process</th><th>Arrival Time</th><th>Burst time</th><th>Priority</th></tr><tr><td>P1</td><td>0</td><td>5</td><td>3</td></tr><tr><td>P2</td><td>1</td><td>3</td><td>2</td></tr><tr><td>P3</td><td>2</td><td>3</td><td>4</td></tr><tr><td>P4</td><td>3</td><td>4</td><td>1</td></tr><tr><td>P5</td><td>4</td><td>3</td><td>5</td></tr></table>	Process	Arrival Time	Burst time	Priority	P1	0	5	3	P2	1	3	2	P3	2	3	4	P4	3	4	1	P5	4	3	5	10
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