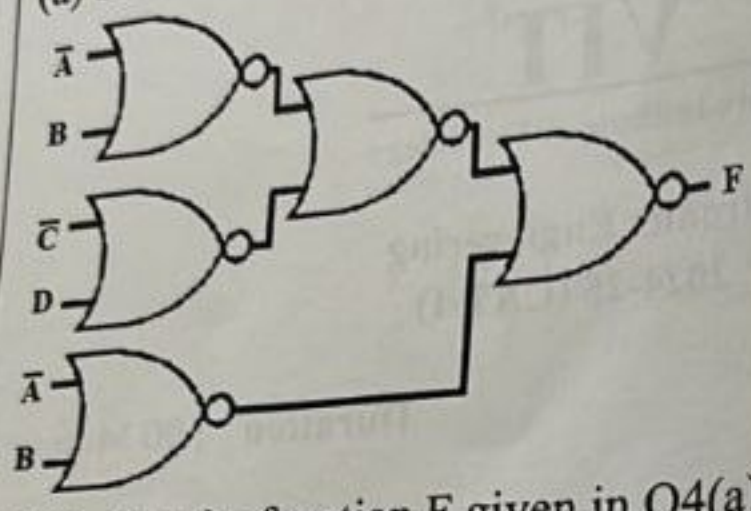
Q4	(a) Sketch the single stage CMOS logic schematic for the given function F.	5



(b) Design the function F given in Q4(a) using transmission gate based multiplexer. 5

Q5	(a) Design the NMOS pass-transistor logic schematic for the expression of sum in full-adder.	5
	(b) Design the PMOS pass-transistor logic schematic for the function shown in the below table. Consider A as control input.	5

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

VIT

Vellore Institute of Technology

School of Electronics Engineering
Fall Semster_2024-25 (CAT-I)

Course Code : BECE303L
Course Name : VLSI System Design
Faculty Name : Dr. Satheesh Kumar S., Dr. Aarthy M., Dr. Antony Xavier Glittas X, Dr. Sandeep Moparthi, Dr. Surya Teja Naga Srinivas P.
Slot : D1

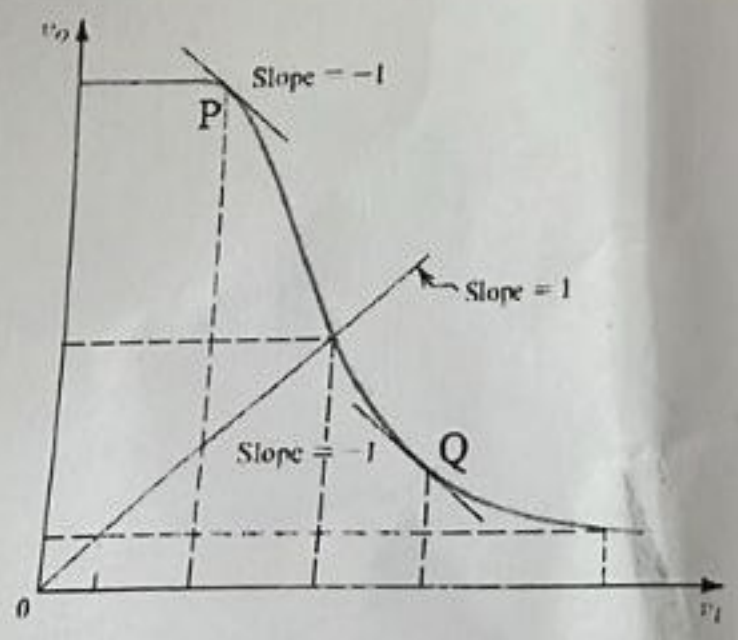
Duration : 90 Minutes
Max. Marks : 50M

Note: $\mathcal{E}_0 = 8.85\ 10^{-12}$ F.m^{-1}, and $\mathcal{E}_{SIO2} = 3.9\ \mathcal{E}_0$

S. No	Question	Marks
Q1	Model the drain current equation of NMOS FET for linear and saturation regions. Incorporate the impact of channel length modulation in the derived expression.	10
Q2	(a) Explain the second order effects in MOSFET resulted from higher electric fields.	4
	(b) Measured data of a MOSFET is given below. Identify the type of the device and solve the parameters β, V_{T0}, and γ. Assume $\varphi_F = -0.25$ V.	6

V_{GS}(V)	V_{DS}(V)	V_{SB} (V)	I_D (μA)
3	3	0	90
5	5	0	357
3	3	2	53
5	5	2	258

Q3	(a) The below figure shows the transfer characteristics of CMOS inverter. Assume the coordinates P(0.7V, 2.1V) and Q(1.4V, 0.15V) are the points on the curve where the slope is -1. Solve the noise margins of the inverter.	5



(b) Solve the expression for output voltage of the CMOS inverter when both pull-up and pull-down are in saturation. 5