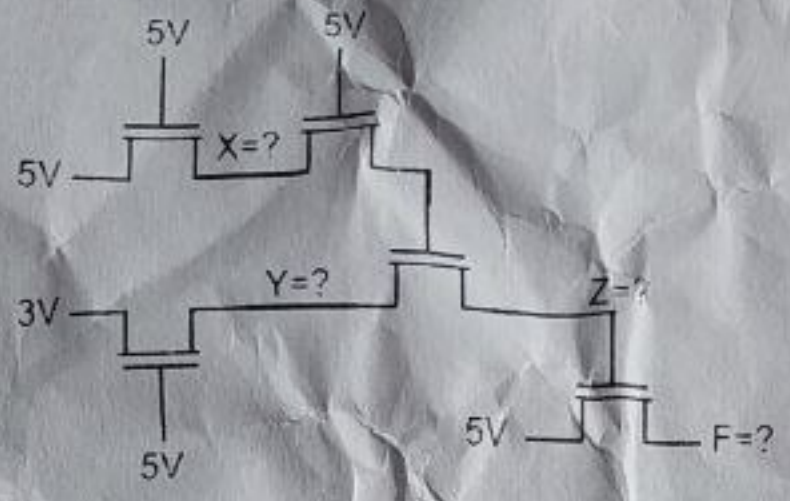
	(b) Estimate the output voltage values for X, Y, Z and F (Assume threshold voltage of all the MOSFETs as 1V) .  	5
Q5	(a) Define noise margins, Evaluate NM_H, Calculate NM_L, when $V_{IH} = 1.6$ V, $V_{IL} = 0.3$ V, $V_{OH} = 1.7$ V and $V_{OL} = 0.2$ V. When a negative 150 mV spike arises at an input voltage of 1.7 V, what is the impact on the circuit? When a negative 150 mV spike arises at an input voltage of 1.7 V, what is the impact on the circuit?	5
	(b) Implement 4×1 multiplexer using 2×1 multiplexer realized using transmission gate logic.	5

22BEC

VIT

Vellore Institute of Technology

School of Electronics Engineering
Fall Semster_2024-25 (CAT-I)

Course Code	: BECE303L	**Duration**	: 90 Minutes.
Course Name	: VLSI System Design		
Faculty Name	: Dr. Satheesh Kumar S, Dr. Aarthy M, Dr. Sri Adibhatla Sridevi, Dr. Antony Xavier Glittas X, Dr. Sandeep Moparthi, Dr. Surya Teja Naga Srinivas P		
Slot	: D2	**Max. Marks**	: 50M

Note: $\varepsilon_0 = 8.85\ 10^{-12}\ F.m^{-1}$, and $\varepsilon_{SiO2} = 3.9\ \varepsilon_0$

S. No	Questions	Marks
Q1	(a) Derive an expression for the output voltage of the CMOS inverter in terms of the input voltage and other device parameters, which is operating in "B" region of operation.	7
	(b) For the nMOS and pMOS transistors: $\beta_n = 2\ \beta_P = 1\ mA/V^2 \cdot V_{Tn} = \lvert V_{Tp} \rvert = 0.4\ V$ and supply voltage = 3V. Calculate the output voltage for the CMOS inverter when input voltage is equal to 0.6V.	3
Q2	(a) Examine the region of operation of pMOS and evaluate drain current for the following bias voltages: $V_{GS} = -2.5\ V$, $V_{DS} = -1.1\ V$, Assume $\beta_P = 60\ mA/V^2$, $V_{TO} = -0.9\ V$, and $\lambda = -0.1V^{-1}$.	4
	(b) Write a short note on Channel Length Modulation, Mobility degradation and Body Effect.	6
Q3	(a) Consider a n-channel MOSFET with t_{ox} =5nm, L=0.5µm, W=1µm, L_{ov} =0.005µm (Length of Overlapping of Gate over Source/Drain Regions). Estimate the following capacitances C_{gb}, C_{gs}, C_{gd} when the MOSFET is operating in saturation region.	6
	(b) Explain CV characteristics with neat diagram in different regions of operation.	4
Q4	(a) The following figure shows a simple logic function realized with logic gates. Implement the function Z using static CMOS as a one stage "Complex Gate". A maximum of 12 transistors is allowed.	5