Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

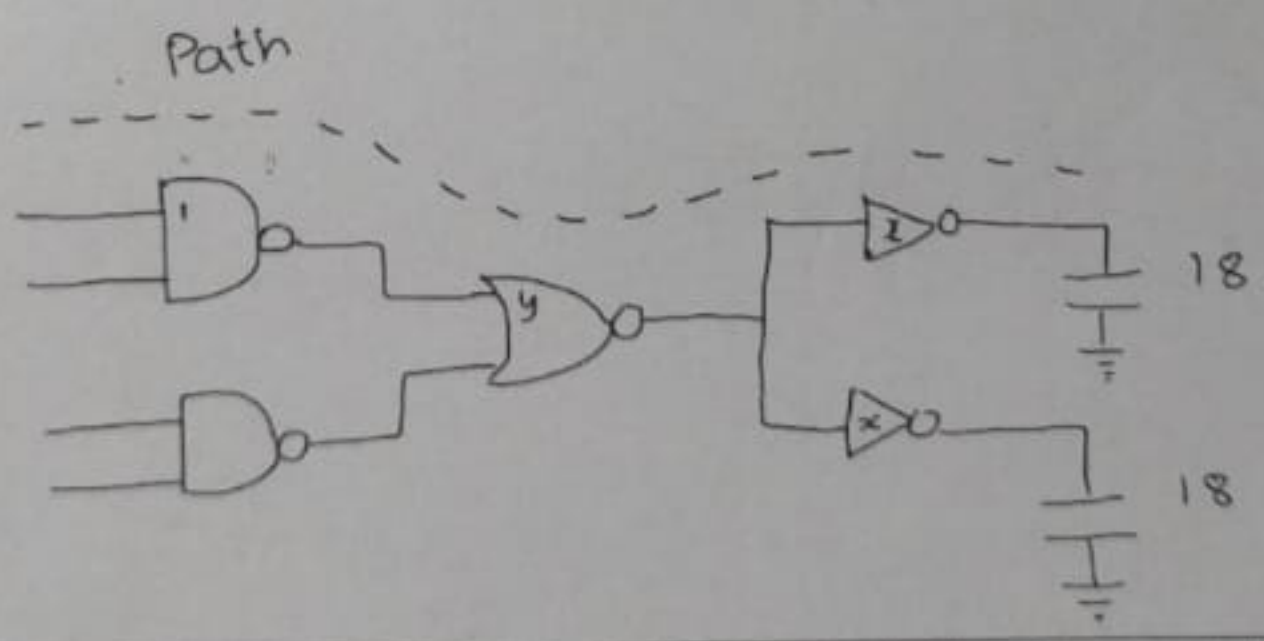
SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2024-2025

SLOT: D2 + TD2

Programme Name & Branch	**: B. Tech & Electronics and Communication**
Course Code and Course Name	**: BECE303L & VLSI system design**
Faculty Name(s)	**: SATHEESH KUMAR, AARTHY, ANTONY XAVIER GLITTAS, SRI ADIBHATLA SRIDEVI, SURYATEJANAGASRINIVAS, SANDEEP MOPARTHI**
Class Number(s)	**: 2876, 2889, 2872, 2898, 2930, 2893**
Date of Examination	**: 16/10/2024**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)
  Apply CMOS technology-specific layout rules in the placement and routing of Transistors and interconnect (CO3).
  Analyse the various logic families and efficient techniques at circuit level for improving power and speed of combinational and sequential logic (CO4).

Q. No	Question	M	CO	BL
Q1	i) Implement the CMOS expression $Y = (ABC + DEF)'$ and size the transistors with respect to the reference inverter sizing Wp = 2Wn. ii) Derive the best case rise time delay, worst case rise time delay and worst case fall time delay in terms of RC.	**4+6**	**CO4**	**BL3**
Q2	Estimate the delay of the path in the circuit shown below and find the capacitance x and y. The input capacitance of two input NAND gate, two input NOR gate and inverter are 1, y and x respectively. 	**10**	**CO4**	**BL3**
Q3	i) A power source is connected between node 1 and ground, R1 is present between node 1 and node 2, C1 is present between node 2 and ground, R2 is present between node 2 and node 3, C2 is present between	**10**	**CO4**	**BL3**

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	node 3 and ground, R3 is present between node 3 and node 4 and C3 is present between node 4 and ground. R1, R2, R3 are resistance, C1, C2, C3 are capacitance and C1= (2×C2) = (3×C3) = 30nF. The delay from the power source to C3 of the circuit is 800ns. In the above-described circuit consider following cases. If only R2 becomes infinite then the delay from the power source is 300ns, if R3 becomes infinite the delay is 450ns. Find the values of R1, R2 and R3. ii) An input module has 500 individual inverters as input buffers which receives mostly one as input. The total dynamic power consumed by the module is 5mW, operating frequency is 100MHz, the average capacitance at the output of the inverters is 0.33pF and supply voltage is 1.2V. Find the activity factor of the inverter and probability of the input of the inverter being one.			
Q4	Draw the stick diagram for the following expression and estimate the area $F(A,B,C,D) = (A + B + CD)'$.	**10**	**CO3**	**BL3**
Q5	Assume the Pseudo NMOS reference inverter circuit has PMOS' size as 2/3 and NMOS' size as 4/3. Obtain the pseudo NMOS logic circuit for the following expression Y = (AB+CD+EF)'. Find the sizes of the NMOS transistors in the pull-down network and calculate the logical effort and delay of the pseudo NMOS logic circuit.	**10**	**CO4**	**BL3**

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