C/L/TX

Reg. No: 22BECOG97

VIT
Vellore Institute of Technology

Final Assessment Test – November 2024

Course: BECE303L - VLSI System Design
Class NBR(s): 2870 / 2875 / 2888 / 2890 / 2901 Slot: D1+TD1
Time: Three Hours Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

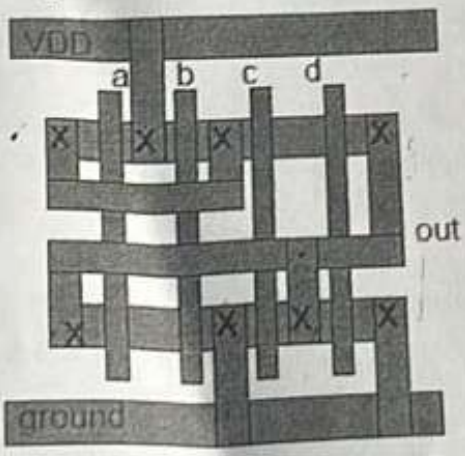
Answer ALL Questions
(10 X 10 = 100 Marks)

1. Determine for each of the measurements the operation region of the transistor (choose from cutoff, resistive and saturated) and the current through the transistor.

NMOS: Kn = 120 μA/V², V_{Tn} = 0.6 V, λ = 0.1 V^{-1},
PMOS: Kp = 30 μA/V², V_{Tp} = –0.6 V, λ = - 0.1 V^{-1}. Assume (W/L) = 1.

	V_{GS} (V)	V_{DS} (V)
NMOS	3.4	2.8
NMOS	0.5	1.2
PMOS	-2.5	-1.8
PMOS	-0.5	-1.2

2. Draw a transistor-level schematic for the stick diagram shown below. Estimate the area of the given stick diagram.

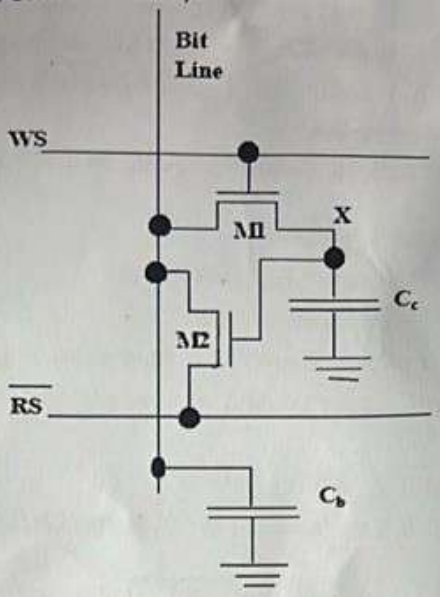


3. Calculate the rise time for the Boolean expression $F = ((AB + C)\,D + E)'$ when the input changes from its initial condition A= 1, B= 0, C=1, D=1 and E=0 to A= 0, B= 0, C=0, D=1 and E=0.

NOTE: size the transistors to get equal rise and fall time and assume no external load, $\beta_n = 2\beta_p$.

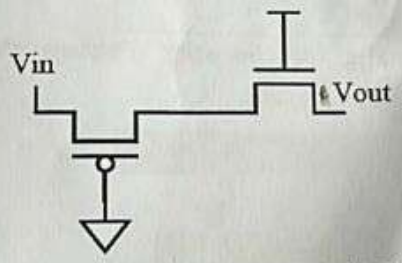
4. The 2-T memory cell shown in figure below, uses 2 identical transistors with W/L = 0.4/0.25. Separate lines are provided for the read select (RS) and write select (WS) signals, which both switch between 0 and 2.5V. The Bit Line is pre-charged to $V_{dd}/2$ prior to a read. A write is done by pulling the bit line either to V_{dd} or to GND. Ignore the body effect and channel-length

modulation. You may assume that k'_n = 115 mA/V², V_{dd} = 2.5 V, V_t = 0.4 V. Explain the operation of the memory.



5. (a) Suppose V_{DD}=1.2 V and V_{tn} =| V_{tp}|= 0.4 V. Determine V_{out} in figure shown below for:

(i) V_{in} = 0 V; (ii) V_{in} = 0.6 V; (iii) V_{in} = 0.9 V; and (iv) V_{in} = 1.2 V. Neglect the body effect.



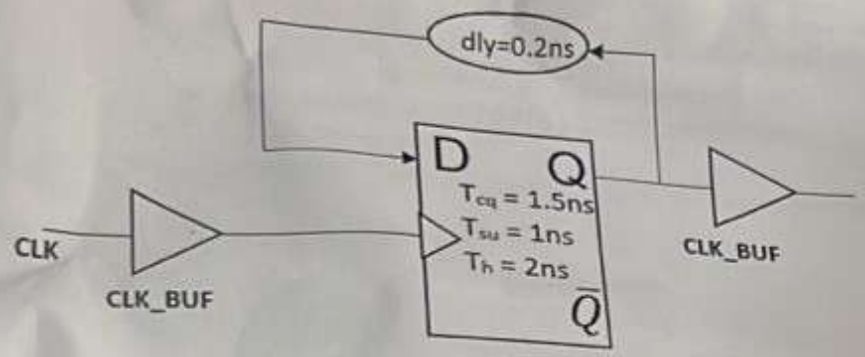
(b) In the transfer characteristics of an inverter, P (1.2V, 2.6V) & Q (1.4, 0.4V) are the points at which the slope is -1. Calculate the Noise Margins (NM_L & NM_H).

6. Explain in detail the CMOS P-well process technology with neat diagrams.

7. Sketch function $F = [A(B + C) + (D)]'$ using each of the following circuit techniques:

(a) CVSL
(b) Domino Logic
(c) Dynamic Logic

8. Consider the circuit diagram and the timing requirement as shown in figure for the flip flop. Two clock buffers are added at the clock pin and the output pin. Also a combination delay of dly = 0.2ns in the input to the output path. Check for any setup/hold timing violation in the circuit with the given timing requirements, and If there is any setup/hold timing violation then what would be the updated value of dly? Also is there any effect on $f_{maximum}$ due to added clock buffers.

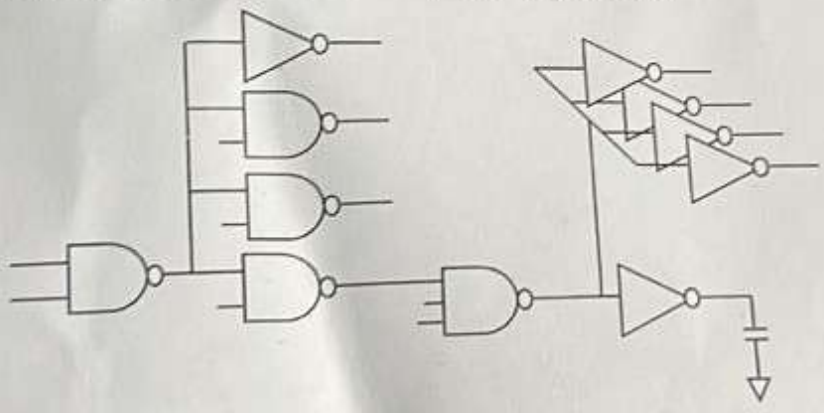


9.(a) Implement Multiplexer based D-Flip Flop and explain its operation with neat timing diagrams.

OR

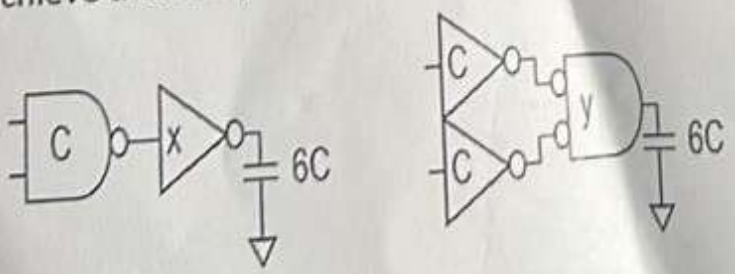
9.(b) Simplify the given Boolean function F(A, B, C, D) = Σm(1, 3, 5, 8, 9, 14, 15) and implement the derived function using (i) CMOS logic with minimum number of transistors. (ii) Transmission gate logic. [7+3]

10.(a) In the figure shown below, calculate the path delay where the input capacitance of the inverter is x, for 2-input NAND gate is 2x and for 3-input NAND gate is 3x. Note: No need to evaluate the value of x.



OR

10.(b) Consider the two designs of a 2-input AND gate shown in figure below. Give an intuitive argument about which will be faster. Back up your argument with a calculation of the path effort, delay, and input capacitances x and y to achieve this delay.



(a) (b)

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