REG.NO.:

VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

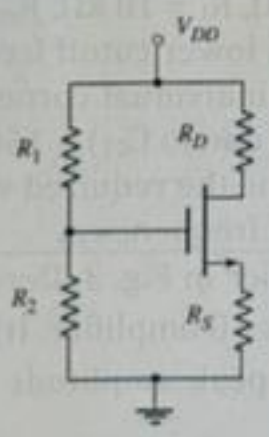
SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
FALL SEMESTER 2025-2026

SLOT:D1+TD1

Programme Name & Branch :B.Tech, ECE
Course Code and Course Name : Analog Circuits-BECE 206L
Faculty Name(s) : Dr. Deepika Rani Sona, Dr. P. Sathyanarayanan, Dr. Gautam Narayan, Dr. Veerapu Goutham, Dr. Pareshkumar Ramanbhai Sagar, Dr. Sandhana Mahalingam M
Class Number(s) : VL2025260100476, VL2025260100480, VL2025260102657 VL2025260100482, VL2025260102667, VL2025260102660
Date of Examination :20.08.2025
Exam Duration : 90 minutes **Maximum Marks:** 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes
  1. Design the BJT and MOSFET amplifier circuits using suitable biasing techniques and analyze their frequency response characteristics.
  2. Distinguish among different classes of MOSFET power amplifiers and employ them for various applications.

Q. No	Question	M	CO	BL
1.	Determine I_D and V_{DS} for the network shown in the figure below with $R_1 = 80\ k\Omega$, $R_2 = 40\ k\Omega$, $R_D = 4\ k\Omega$, $R_S = 1\ k\Omega$. Let $V_{DD} = 12$ V, $V_{tn} = 1.5$ V, $k_n'(W/L) = 2\ mA/V^2$. Plot the load line and Q point parameters for the circuit.  Fig.1	10	1	3
2.	A common-emitter amplifier is biased with a voltage-divider network and is powered from a single supply V_{CC} = +15 V. The circuit parameters are: $R_{B1} = 100\ k\Omega$ (Voltage divider resistor from base to Vcc), $R_{B2} = 27\ k\Omega$ (voltage divider resistor from base to ground), $R_C = 4.7\ k\Omega$, $R_E = 1.0\ k\Omega$, Load resistor R_L = 10 kΩ, Input signal source: V_{sig} with source resistance $R_{Sig} = 600\ \Omega$. Transistor DC parameters: $\beta_F = 120$, Early voltage $V_A = 120$ V. Thermal voltage $V_T = 25$ mV. The amplifier is biased such that at the quiescent point: $I_{CQ} = 2.5$ mA and V_{CEQ} = 7.5 V Assume the coupling capacitors are 1uF and the bypass capacitor is 100 uF. **i).** Draw the circuit diagram. **ii).** Draw the A/C equivalent circuit and the Small-signal A/C equivalent circuit using the hybrid-π model. **iii).** Calculate the small-	10	1	3

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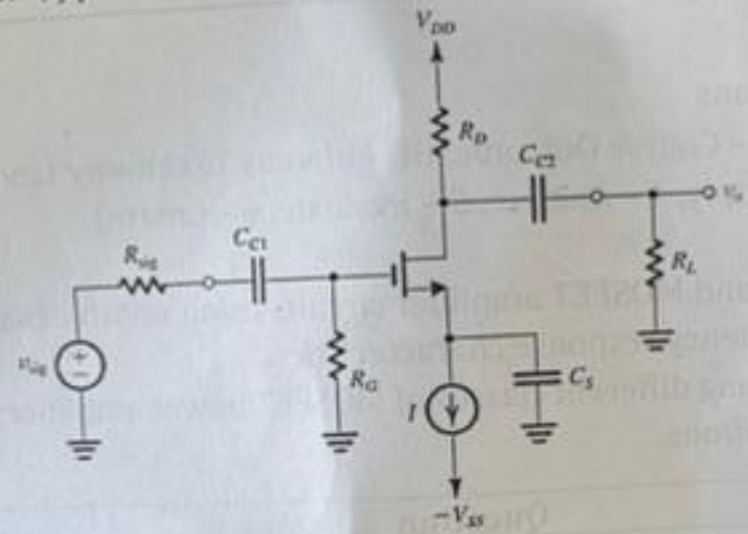
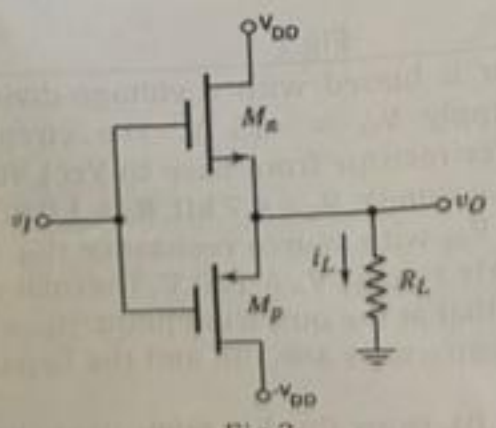
	signal model parameters. **iv).** Derive an expression for the overall mid-band voltage gain. **v).** Recompute the gain assuming the Early effect is negligible (i.e., $r_o \rightarrow \infty$). Compare the two gains (with and without r_o) and comment quantitatively on how the Early effect changes the gain in this amplifier.			
3.	Derive the expression for the upper 3-dB frequency f_H of the common source amplifier as shown in Fig.2 (showing the Miller effect). Compute C_{eq} using the given numerical values. R_{sig}=100kΩ, R_G=4MΩ, C_{gs}=3nF, g_m=2mA/V, r_0=15kΩ, R_D=10kΩ, R_L=25kΩ, f_T=10MHz, and $V_{DD} = V_{SS} = \pm 15V$.  Fig. 2	10	1	3
4.	Consider the single-stage common-emitter amplifier. The circuit parameters are: R_1 = 56 kΩ, R_2 = 10 kΩ, R_C = 4.7 kΩ, R_L = 10 kΩ, R_{sig} = 600 Ω, β = 100, g_m = 40 mS. The designer requires the overall lower cutoff frequency of the amplifier to be f_L(overall) = 500 Hz. The desired individual corner frequencies contributed by each capacitor are specified as f_{L1} (due to C_{C1}) = 150 Hz, f_{L2} (due to C_{C2}) = 150 Hz, f_{L3} (due to C_E) = 200 Hz. Determine the required values of C_{C1}, C_{C2} and C_E to achieve the specified individual cutoff frequencies.	10	1	3
5.	**i).** Consider the class-B power amplifier in Fig. 3. Derive the equation for power conversion efficiency of the given class-B amplifier. **ii).** Let V_{DD}=6V and R_L=40Ω. If the output is sinusoid with 2.4V peak amplitude then calculate the power conversion efficiency.  Fig.3	10	2	3