REG.NO.:

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

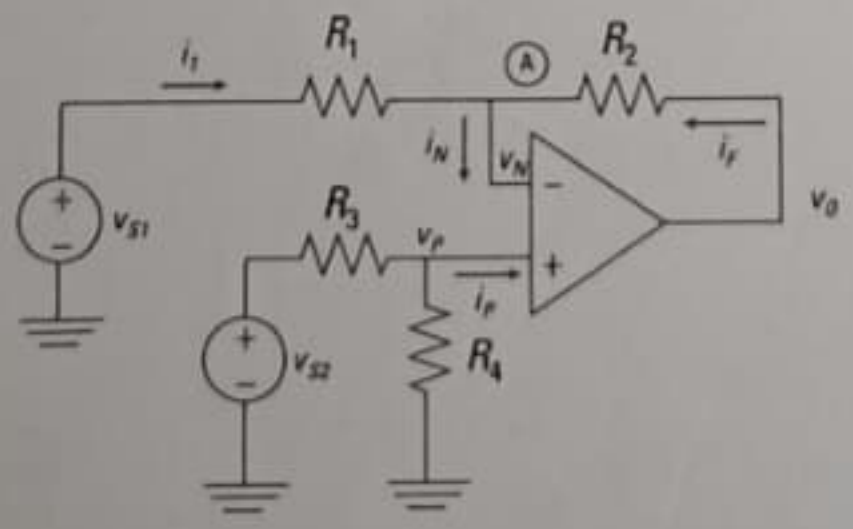
SLOT:D1+TD1

Programme Name & Branch :B.Tech, ECE
Course Code and Course Name : Analog Circuits-BECE 206L
Faculty Name(s) : Dr. Deepika Rani Sona, Dr. P. Sathyanarayanan, Dr. Gautam Narayan, Dr. Veerapu Goutham, Dr. Pareshkumar Ramanbhai Sagar, Dr. Sandhana Mahalingam M
Class Number(s) : VL2025260100476, VL2025260100480, VL2025260102657 VL2025260100482, VL2025260102667, VL2025260102660
Date of Examination : 8.10.2025
Exam Duration : 90 minutes **Maximum Marks:** 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes

3. To introduce MOSFET active biasing and design a MOSFET differential amplifier circuit and analyze its frequency response.
4. To study the characteristics of Operational Amplifier and its applications
5. To acquaint and demonstrate the concepts of waveform generators, filter configurations, Timer, data converters, and Voltage regulators.

Q. No	Question	M	CO	BL
1.	For the MOS differential pair with a common-mode voltage V_{cm} is applied. Let $V_{DD} = V_{SS} = 12V$, $V_t = 0.8V$, $V_{OV} = 0.6V$, $\mu_n C_{ox} = 4\,mA/V^2$, $W/L = 2$, $R_D = 7K\Omega$, and neglect channel-length modulation. (a) Find $I$and V_{GS} (b) For $V_{cm} = -2V$, find V_S , I_{D1} , I_{D2} , V_{D1}, and V_{D2} (c) What is the highest permitted value of V_{cm} for which the transistors remain in saturation? (d) For $V_{cs} = 0.7V$, what is the lowest value of V_{cm} for which the transistors remain in saturation?	10	3	3
2.	(a) For the op-amp circuit shown in Fig.1, use the following values: $V_{S1} = 3V$, $V_{S2} = 1V, R_1 = 10k\Omega$, $R_2 = 40k\Omega$, $R_3 = 10k\Omega$, $R_4 = 10k\Omega$. Calculate the output voltage V_O.  Fig.1	4 + 6	4	3

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	(b) Design an ideal op-amp inverting differentiator with a differentiation time constant of 10^{-2} s and an input capacitance of 0.01 μF. What is the gain magnitude and phase of this circuit at 10 rad/s, and at 10^3 rad/s ?.			
3.	(a) For the non-inverting amplifier, R_1 = 2 kΩ, and R_f = 15 kΩ. Calculate the maximum output offset voltage due to V_{ios} and I_B. The op-amp is LM307 with V_{ios}= 15 mV and I_B = 380 nA, I_{os} = 45nA.		4	3
	(b) Determine the maximum possible change in output offset voltage in an inverting amplifier R_1 = 1kΩ, R_f = 100kΩ after 28 days if the op-amp is the μA741 with the following specification $\frac{\Delta V_{io}}{\Delta t} = 35\mu V/week$ and $\frac{\Delta I_{io}}{\Delta t} = 0.5nA/week$. Assume that the circuit is initially nulled at that room temperature and the voltage across terminals $+V_{CC}$ and $-V_{EE}$ remains constant.	5 + 5		
4.	Refer to the circuit shown in Fig. 2. Using the given parameters, determine the waveform that would appear on Oscilloscope Channel A. Calculate the output signal time period and the hysteresis voltage.	10	5	3
5.	Design an op-amp squarewave generator powered from a ±12 V supply to generate a rectangular wave with the following specifications: output frequency = 1.00 kHz and duty cycle = 75%.	10	5	3

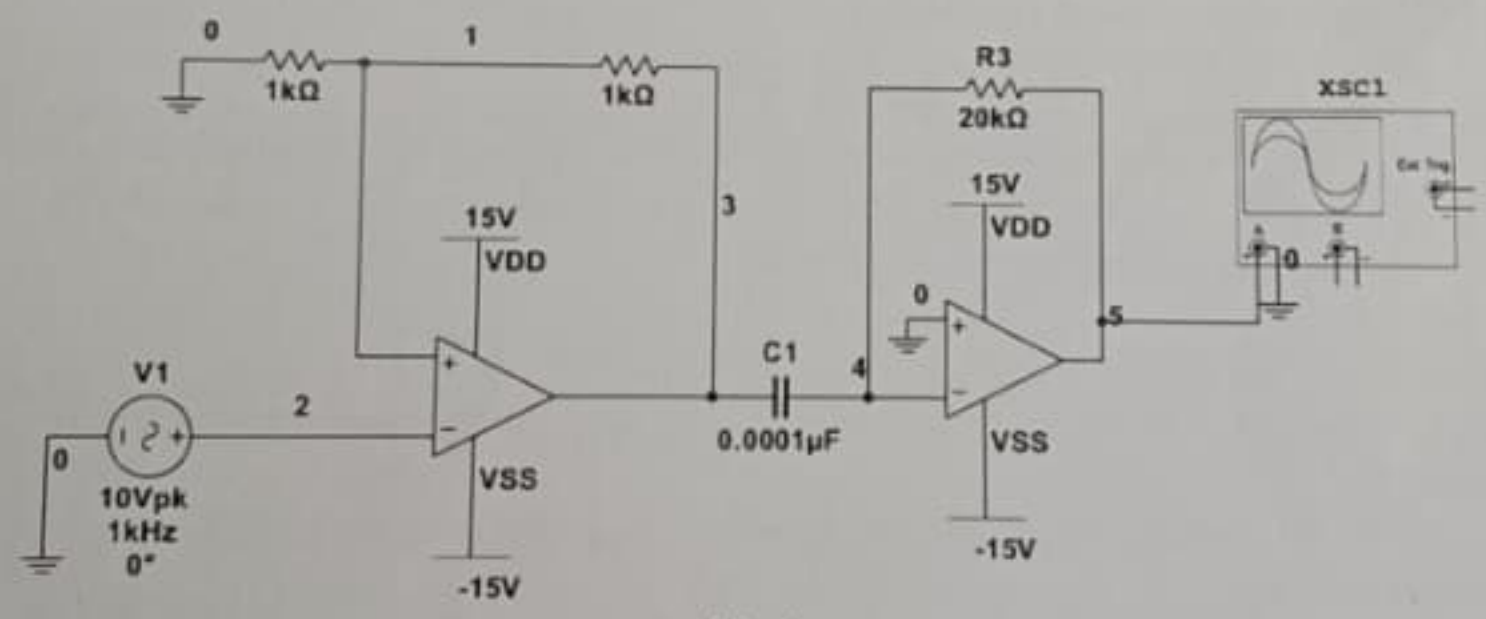

Fig.2