Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRICAL ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2025-2026

Programme Name & Branch	**: B.Tech (EEE & EIE)**
Course Code and Course Name	**: BEEE208L – Analog Electronics**
Faculty Name(s)	**: Dr.M.N. Venkataraman, Dr.R. Gnanavignesh**
Class Number(s)	**: VL20252601012345, 2253**
Date of Examination	**: 15/03/2026**
Exam Duration	**: 90 minutes**

General instruction(s): **Maximum Marks: 50**

- Answer All Questions.
- Rough work should not be done on the question paper. It will be treated as malpractice.
- M – Max mark; CO – Course Outcome; BL – Bloom's Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Course Outcomes Statements:

CO. 3. Design the frequency of oscillation for different oscillators.

CO. 5. Design ADCs, DACs and timer circuits for engineering applications.

Q. No	Question	M	CO	BL
1.	Draw the complete circuit of Hartley oscillator and obtain the frequency of oscillation.	10	3	3
2.	Design a 4-bit R-2R resistor type DAC whose feedback resistor value is 2.5kΩ. Draw the complete circuit diagram with the exact components.	10	5	4
3.	Design a 4-bit flash ADC inclusive of the priority encoder with a clear diagram.	10	5	4
4.	Design a monostable multivibrator with T_{ON}=1ms and using 555- Timer. Use 1μF capacitor. Draw the circuit and explain your design including the 555-Timer internal diagram.	10	5	3
5.	Design a adjustable regulator for voltage supply of 8V from voltage regulator using IC7805.	10	5	2