REG.NO.:

SLOT:D1+TD1

VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
FALL SEMESTER 2025-2026

Programme Name & Branch : B.Tech. CSE
Course Code and Course Name : BACSE103 - Computation Structures
Class Number(s) : 7232/7234/7238/7241/7244/7245/7249/7251/7253/ 7240/7302/7304/7306/7311/
Date of Examination : 20.08.2025
Exam Duration : 90 minutes **Maximum Marks:50**

General instruction(s):

- Answer All Questions
- M- Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply,4 – Analyse,5 – Evaluate,6 – Create)
- Course Outcomes
  1. To design and optimize minimal combinational circuits.
  2. To analyze and design sequential circuits utilizing various types of flip-flops.

Q.No	Question	M	CO	BL
1.	a) Imagine you're designing a digital clock that also displays temperature. You measure a room temperature of 35.625°C using a sensor. Convert this room temperature into the format of displays given below: □ The microcontroller converts it to binary to store in memory. □ The octal format is used because the 7-segment display driver supports octal-coded inputs. □ The hexadecimal format is used when sending the value to a computer through USB, as it's more compact and readable.	5	1	4
	b) Determine the value of the radix "r" in the number $(121)_{(r)}$ such that its decimal equivalent is equal to $(100)_{10}$.	5	1	4
2.	a) Simplify the following Boolean function using Karnaugh Map (K-Map) and implement the simplified expression using basic 2-input logic gates: **$F(A, B, C, D) = \Sigma_m(0, 2, 3, 5, 6, 7, 8, 10, 12, 14)$.**	6	1	5
	b) To promote a creative usage of existing components and building foundational logic design skills in a school-level digital electronics project where students are asked to build logic circuits for a full adder using a 3:8 decoder instead of using complex logic gates. Specify the Min-terms of the full adder and design it.	4	1	6
3.	Design a combinational circuit to implement the Boolean function **$F(A, B, C, D) = A \cdot B. C + A' \cdot C \cdot D + B \cdot C' \cdot D$** using a **4:1 multiplexer**. Note: Use variables **C** and **D** as the selection lines.	10	1	6

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4.	You're building a 4-bit calculator as part of your first-year digital logic lab. The calculator should perform the binary addition of two 4-bit numbers. i) Implement the addition logic using a 4-bit Ripple Carry Adder. When you input values like 0110 (6) and 0101 (5), the output appears correctly. ii) However, when adding larger binary numbers like 1111 (15) and 1111 (15) using Ripple Carry Adder logic, you observe a delay in obtaining the final output. Design a suitable combinational logic circuit to overcome this delay.	10	1	6
5.	Explain in detail the operation of SR and JK, flip-flops with truth tables, characteristic table and logic diagrams. Highlight the use of JK flip-flop in edge-triggered sequential circuits.	10	2	2

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