SCHOOL OF COMPUTER SCIENCE ENGINEERING AND INFORMATION SYSTEMS

CONTINUOUS ASSESSMENT TEST - I

FALL SEMESTER 2025-2026

SLOT: F1+TF1

Programme Name & Branch : B.Tech – Computer Science and Engineering-Artificial Intelligence and Data Engineering/ Cyber Security

Course Code and Course Name : BACSE103 & Computation Structures

Faculty Name(s) :Dr.MALASERENE I, Dr. KRISHNAMOORTHY N, Dr.DEEPA M Dr. BALAJI E

Class Number(s) : VL2025260105815, 817, 824, 826

Date of Examination : 22-Aug-2025

Exam Duration : 90 minutes **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- CO1: To design and optimize minimal combinational circuits.
- CO2: To analyze and design sequential circuits utilizing various types of flip-flops

Q. No	Question	M	CO	BL
1.	a) Convert the following decimal numbers to binary numbers 19.25 **(2 marks)** b) Convert the hexadecimal number $(4FB2)_{16}$ into its octal equivalents. Show all intermediate steps in your conversion. **(2 Marks)** c) Convert the following decimal numbers to hexadecimal numbers 125.8125 (Limit fractional part to 3 digits). **(2 Marks)** d) Using only 2-input NAND gates, implement the two Boolean functions below. You must show all derivation steps, provide gate-level diagrams, and justify your designs. **(4 Marks)** F1(A,B)=A+B F2(A,B)=A·B	10	1	2
2.	**(a)** The Boolean function is given in Sum of Products (SOP) form as: **F(A,B,C,D)=A′B′C′D′ + A′BC′D + AB′C′D + AB′CD + ABCD′ + A′BCD** Using a 4-variable Karnaugh Map (K-map), simplify the above function to obtain the minimal SOP expression. Then, draw the logical circuit diagram for the simplified SOP form using only AND, OR, and NOT gates. **(5 Marks)** (b) Using the same K-map, determine the minimal Product of Sums (POS). Then, draw the logical circuit diagram for the simplified POS form using only OR, AND, and NOT gates. **(5 Marks)**	10	1	4

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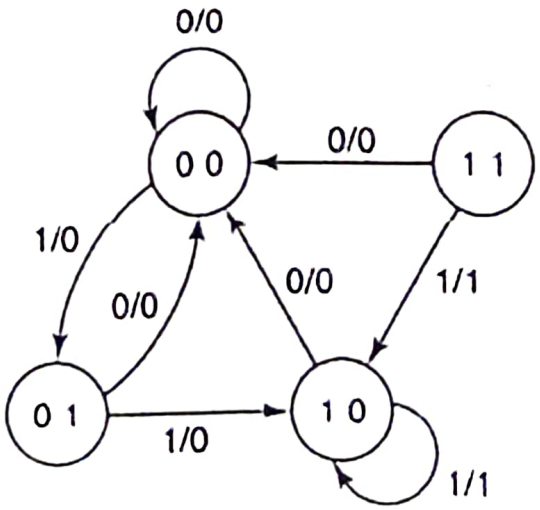
3.	A company is developing a digital weighing machine that can compare the weight of two items placed on two different pans. The machine must display whether the left pan is heavier, lighter, or equal in weight compared to the right pan. The weight values are represented in binary form, and the comparison is done by subtracting the right pan value from the left pan value for each corresponding bit, considering any borrow from the previous stage. To implement this feature: (a) Design a Combinational circuit that takes three inputs: Write the truth table for the above circuit and derive the simplified Boolean expressions for D and Bout using K-map simplification. **(6 Marks)** (b) Implement the logic circuit diagram of the Full Adder using 3x8 Decoder. **(4 Marks)**	10	1	3
4.	a) A self-service vending machine has 8 different snack items, each assigned a unique number from 0 to 7. When a customer presses a button for a snack, only one button is active at a time, and the machine needs to send the selected snack number to the control system in binary code. To achieve this: Design an 8-to-3 circuit that takes 8 input lines (I_0 to I_7) corresponding to the snack buttons and produces a 3-bit binary output (Y_2, Y_1, Y_0). Write the truth table for the circuit. And Draw the logic circuit diagram for the 8-to-3 circuit using basic gates. **(6 Marks)** b) Implement the function F (A, B, C) = $\sum$ (1, 2, 6, 7) using with a 4-to-1 line MUX. **(4 Marks)**	10	1	4
5.	Find the state table and design a synchronous sequential circuit using JK flip flop for the following state diagram shown below  	10	2	5

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