VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SLOT: D2+TD2

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

Programme Name & Branch	: B.Tech & Computer Science and Engineering
Course Code and Course Name	: BACSE103 & Computation Structures
Faculty Name(s)	: Dr. Gayathri S, Dr. R. Banupriya, Dr. Muchenedi Hari Kishor, Ms. Preethi Sudha, Dr. Gerardine Immaculate Mary, Dr. Karthikeyan A, Dr. Vani Rajasekar, Mr. Prabhu R, Mr. Soumyajyoti Dey, Mr. Ch Ramesh Babu, Dr. Prabin Jose J, Dr. Satyajit Mohanty
Class Number(s)	: VL2025260107252, VL2025260107303, VL2025260107308 VL2025260107233, VL2025260107242, VL2025260107250, VL2025260107246, VL2025260107305, VL2025260107239 VL2025260107254, VL2025260107262
Date of Examination	: 08.10.2025
Exam Duration	: 90 minutes

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyze, 5 – Evaluate, 6 – Create)
- Course Outcomes (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)
  2: To analyze and design sequential circuits utilizing various types of flip-flops.
  3: To analyze different instruction formats, addressing modes and validate efficient algorithms for fixed-point arithmetic operations

Q. No	Question	Module	Marks	CO	BL
1.	A group of flip flop needs to send 4-bit data to another device, but it only has one data line available. Which type of shift register would be most suitable for the cases given below and explain each of them in detail. CASE 1 : It loads 4-bit data in parallel, then shifts it out bit-by-bit through a single line. CASE 2: It collects serial bits and converts them back to parallel form.	2	10	2	3

2.	In an Elevator Safety System, the elevator should not move beyond the 4th floor. How can a counter be used asynchronously? Each floor movement generates a pulse and then the counter increments. After 4 counts, the counter resets, triggering the next signal change. Find the timing sequences for both up counting as well as down counting. Ripple delay is acceptable since elevators move slowly.	2	10	2	4
3.	a) A smartphone uses a type of processor architecture where instructions and data share the same memory bus. How could the memory unit of this architecture will be allocated for the data word and instruction word? Suggest one possible architectural improvement to reduce the performance problem when the phone is running multiple applications.	3	5	3	2
	b) Differentiate the scenario when Single memory is used for instructions and data with separate memory for holding the instructions and data in the aspect of performance, memory access, modification of data and explain how the data can be shared in both the cases and state the applications where those architectures are used.	3	5	3	2
4.	a) A processor's ALU is designed to perform binary division using the restoring division method. If the dividend is 1001_2 (9 in decimal) and the divisor is 010_2 (2 in decimal), trace the restoring division steps. Show the final quotient and remainder.	3	5	3	4
	b) Compare and contrast the architectures that executes an instruction in a single clock cycle while the other one executes an instruction in multiple clock cycle.	3	5	3	4
5.	A CPU executes multiple instructions in a pipeline. Identify each phase of an instruction cycle that starts from the address calculation of an instruction to store the results. With a neat sketch explain all the phases in detail.	3	10	3	2

****