VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.: 25BVD0126

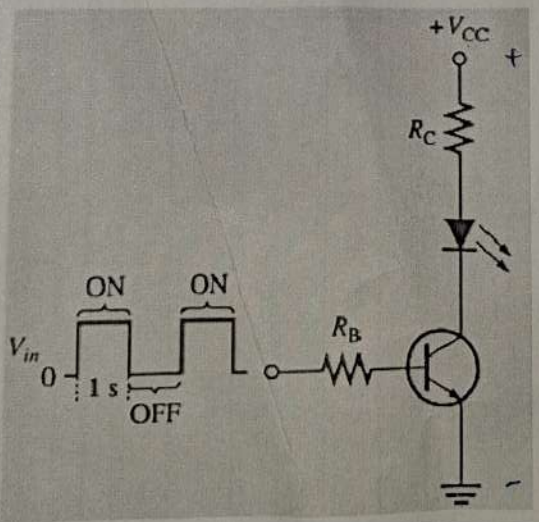
SCHOOL OF ELECTRONICS
CONTINUOUS ASSESSMENT TEST - 2
WINTER SEMESTER 2025-2026

SLOT: A2+TA2

Programme Name & Branch : B.Tech. Electronics Engineering(VLSI Design and Technology)
Course Code and Course Name : BAEVD101 & Electronic Devices
Class Number (s) : VL2025260500815
Faculty Name (s) : Dr. Shelja
Exam Duration : 90 Min.
Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes: Employ the semiconductor fundamentals to homo- and hetero-semiconductor junctions and electronic devices

Q.No.	Question	M	CO	BL
1.	The LED in the figure emits sufficient light when the collector current reaches the required operating value. For the following circuit values, $V_{CC} = 9V, R_C = 220\Omega, R_B = 3.3k\Omega, \beta = 50, V_{CE(sat)} = 0.3V, V_{LED} = 1.6V$ (a) Determine the collector current when the transistor is in saturation. (b) Calculate the minimum base current required to drive the transistor into saturation. (c) Using twice the minimum base current as a safety margin, determine the minimum amplitude of the square-wave input voltage V_{in} required to ensure saturation. (d) If the input square-wave amplitude is V_{in} = 5V and 6V, will the LED glow sufficiently? Justify your answer with calculations. 	15	CO2	BL4

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2.	A silicon npn BJT has common emitter current gain of 150 with reverse saturation current of 5×10^{-16} A in emitter base junction. The early effect voltage is 120 V at 300K. It is biased at V_{BE} = 0.68 V is very large than V_{BC}. a. Find out the collector current I_C in BJT using ebers moll model. b. Also draw the equivalent hybrid π model and find g_m, r_π, r_o.	10	CO2	BL3
3.	A silicon MOS structure has the following parameters: ▪ Metal gate work function, $\Phi_M = 4.8$ eV ▪ Electron affinity of silicon, $\chi_{Si} = 4.05$ eV ▪ Energy difference between conduction band and Fermi level in the substrate, $(E_C - E_F) = 0.30$ eV ▪ Oxide thickness, $t_{ox} = 12$ nm ▪ Substrate doping (p-type): $N_A = 5 \times 10^{16}$ cm^{-3} ▪ Oxide charge components: $Q_f = 5 \times 10^{-9}$ C/cm^2, $Q_{ot} = 4 \times 10^{-9}$ C/cm^2, $Q_{it} = 2 \times 10^{-9}$ C/cm^2, $Q_m = 1 \times 10^{-9}$ C/cm^2 Assume Relative permittivity's: $\varepsilon_{ox} = 3.9\varepsilon_0$, $\varepsilon_{si} = 11.7\varepsilon_0$, at $T = 300$ K and $V_T = 26$ mV. Find: a. Work function difference Φ_{MS} b. Total oxide charge density Q_{ox} c. Flat-band voltage V_{FB} d. Threshold voltage V_{TH} e. Draw the Energy Band Diagram (EBD) of the MOS capacitor at flat-band condition and strong inversion (label $E_C, E_V, E_F, \Phi_M, \Phi_S$).	15	CO3	BL3
4.	A p-type MOS capacitor has the following parameters: • Oxide thickness $t_{ox} = 15$ nm • Substrate doping $N_A = 2 \times 10^{16}$ cm^{-3} • Fermi potential: $\phi_F = 0.36$ V • $\varepsilon_{ox} = 3.9\varepsilon_0$, $\varepsilon_{si} = 11.7\varepsilon_0$ • Gate area $A = 100\ \mu$m $\times 100\ \mu$m • $n_i = 10^{10}$ cm^{-3}, $T = 300$ K Calculate: i. Oxide capacitance per unit area C_{ox} ii. Maximum depletion width $W_{d,max}$ iii. Minimum capacitance C_{min} Also draw the low-frequency C–V characteristics of the MOS capacitor and clearly mark Accumulation, depletion, and inversion regions.	10	CO3	BL4