VIT
Vellore Institute of Technology

REG.NO.:

SLOT:G2+TG2

SCHOOL OF COMPUTER SCIENCE ENGINEERING AND INFORMATION SYSTEMS
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2025-2026

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|---|---|---|
| Programme Name & Branch | : B.Tech(IT) | |
| Course Code and Course Name | : BITE301L&Computer Architecture and Organization | |
| Faculty Name(s) | : Prof: SUMATHY.S, | Prof: SUMATHI .D, |
| | Prof:KRISHNAMOORTHY N, | Prof:MEENACHI.S |
| ClassNumber(s) | :VL2025260502758, | VL2025260502756, |
| | VL2025260502755 | VL2025260502751, |
| Date of Examination | :23 03-2026 | |
| Exam Duration | : 90 minutes | Maximum Marks: 50 |

General instruction(s):

- Answer All Questions
- M - Max mark; CO - Course Outcome; BL - Blooms Taxonomy Level (1 - Remember, 2 - Understand, 3 - Apply, 4 - Analyse, 5 - Evaluate, 6 - Create)
- Course Outcomes

CO2:Design instruction level parallelism using instruction stages. Understand pipelining concepts and identify the hazards to rectify in typical processer pipeline

CO3:Analyse the arithmetic algorithms to perform ALU operations.

CO4:Design a memory system on understanding the chip organization and analyse its performance

| Q. No | Question | M | CO | BL |
|---|---|---|---|---|
| 1. | Assume that each word occupies 4 bytes of memory. The initial value of the Stack Pointer (SP) is 40. The base address of array D is 300. The array D contains four elements: 14, 6, 9, and 2. The number of elements in the array (N) is 4. Consider a following program in which the base address of array D and the value of N are passed to a subroutine using the stack for further processing. | 10 | CO2 | 3 |

| Main Program | |
|---|---|
| 1) Move #D, -(SP) | 11) **INNER:** Move (R3), R0 |
| 2) Move N, -(SP) | 12) Move 4(R3), R5 |
| 3) Call **SORTSUB** | 13) Compare R5, R0 |
| 4) Add #8, SP | 14) Branch>= **SKIP** |
| 5) **SORTSUB**: MoveMultiple R0-R4, -(SP) | 15) Move R5, (R3) |
| 6) Move 24(SP), R1 | 16) Move R0, 4(R3) |
| 7) Move 28(SP), R2 | 17) **SKIP:** Add #4, R3 |
| 8) Decrement R1 | 18) Decrement R4 |
| 9) **OUTER:** Move R1, R4 | 19) Branch>0 **INNER** |
| 10) Move R2, R3 | 20) Decrement R1 |
| | 21) Branch>0 OUTER |
| | 22) MoveMultiple (SP)+, R0-R4 |
| | 23) Return |

| | | | | |
|---|---|---|---|---|
| | a)What is the value of SP and content of SP after execution of Line 1?<br>(b) What are the contents of stack memory and value of SP after execution of Line 8?<br>(c) What are the values of R0, R1, R2, R3, R4and R5 after execution of Line 13 during the first INNER loop?<br>(d) What are the values of R0, R1, R2, R3, R4 and R5 after the second comparison in the INNER loop?<br>(e) What is the final sorted array after completion of the program? | | | |
| 2. | Perform Signed Magnitude division on 18 and 4 using Restoring Binary division algorithm. | 10 | CO3 | 2 |
| 3. | Show the step by step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 6-bit registers that hold signed numbers. (-19) x (+16) | 10 | CO3 | 4 |
| 4. | Consider three floating-point numbers **A, B, and C** stored in registers **Ra, Rb, and Rc,** respectively, according to the **IEEE 754 single-precision floating-point format**.<br><br>he 32-bit hexadecimal values stored in the registers are:<br><br>Ra = 0xC1400000 Rb = 0x42100000 Rc = 0x41400000<br><br>Answer the following:<br><br>1. Convert each IEEE-754 single-precision number into its decimal equivalent by identifying the sign bit, exponent, and mantissa.<br><br>2. Using the obtained decimal values of A, B, and C, verify the correctness of the following expressions:<br><br>a) A + C = 0 b) B = 3C c) (B − C) > 0<br><br>3. Show all intermediate steps involved in the conversion and verification | 10 | CO3 | 4 |
| 5. | Design **512 × 16-bit RAM** using **256 × 8-bit RAM chips**. Also design **512 × 8-bit ROM** using **256 × 8-bit ROM chips**.<br><br>To find:<br><br>a) Determine number of chips required<br>b) Draw the memory organization diagram<br>c) Show address line connections and chip select logic.<br>d) Draw the block diagram / chip layout for the above memory organization. | 10 | CO4 | 2 |