



SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

Programme Name & Branch : B. Tech & CSE
Course Code and Course Name : BACSE103 and COMPUTATION STRUCTURES
Class Number(s) : 7257/7259/7261/7263/7265/7269/7309
Date of Examination : 07/10/2025
Exam Duration : 90 minutes
Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO - Course Outcome; BL - Blooms Taxonomy Level (1 - Remember, 2 - Understand, 3 - Apply, 4 - Analyse, 5 - Evaluate, 6 - Create)
- Course Outcomes (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)
 1. To design and optimize minimal combinational circuits.
 2. To analyze and design sequential circuits utilizing various types of flip-flops.
 3. To analyze different instruction formats, addressing modes and validate efficient algorithms for fixed-point arithmetic operations

Q. No	Question	Module	Marks	CO	BL
1.	The next-state minterms are provided below, where A and B denote the present-state and x is the input. $DA(A, B, x) = \sum(1, 3, 5, 7)$ $DB(A, B, x) = \sum(2, 3, 6, 7)$ $y(A, B, x) = \sum(2, 5)$ a) Construct the state table, and derive the state equations as well as the output equation. b) Draw the logic diagram of the circuit using only D flip-flops and logic gates. c) Draw the state diagram with all states. d) Identify whether the circuit represents a Mealy model or a Moore model, and justify your answer briefly.	2	10	2	3
2.	i) A communication system needs to transmit a 5-bit data word 10111 using two different methods: Scenario A - Data bits are entered one at a time, and with every clock pulse each bit shifts to the next stage until it appears at the output. Scenario B - The 5-bit word is first loaded into a register in a single clock pulse, after which the bits are sent out one by one on successive clock pulses. Explain how the data is handled in each method with respect to loading and transmission. Calculate the number of clock pulses required in both methods for transmitting the complete 5-bit word. Which method would be more suitable if the priority is fast loading, and why?	2	6	2	



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	ii) A vending machine is designed to release a product only after it detects 10 coins inserted one by one. To implement this, a counter circuit is used that advances its count with every clock pulse generated by the coin sensor. Once the count reaches 10, the counter resets automatically and sends a signal to release the product. Explain how such a counter works in this application. Show the sequence of counts that occur and what happens after the 10th input pulse?	2	4	2	4
3.	Multiply 16×-7 using Booth's and bit pair recoding algorithm. Show all steps including binary representation of both numbers and the sequence of partial products.	3	10	3	3
4.	In restoring division, explain what happens when the partial remainder becomes negative during the division process. Demonstrate the step-by-step procedure of restoring division $73/4$ showing all intermediate steps, including the handling of a negative partial remainder.	3	10	3	3
5.	i) Write an appropriate assembly language program for the following operation and interpret it according to the Von Neumann IAS architecture. The memory locations are assigned as follows: $a \rightarrow 801, b \rightarrow 802, c \rightarrow 803, d \rightarrow 804, y \rightarrow 805$ The expression is: $y = ((a + b) \times (c - d)) + ((a \times c) - (b \times d))$	3	6	3	4
	ii) Write an appropriate assembly language program to perform multiplication of three numbers using immediate and indirect addressing modes. The expression is: $z = a * b * c$ a) Show clearly how immediate and indirect addressing modes are used in the program when the values of $a=5, b=2, c=3$. b) Explain the concept of immediate addressing mode and indirect addressing mode and draw the block diagram representation of both addressing modes, clearly indicating how the operand is accessed in each case.	3	4	3	4