VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SLOT: C2 + TC2

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

Programme Name & Branch : B. TECH
Course Code and Course Name : BACSE103, COMPUTATION STRUCTURES
Faculty Name(s) : Dr. SUKANTA GHOSH, Dr. VIJAYA DURGA CHINTALA, Dr. ANIS FATEMA, Mr. JIM SOLOMON RAJA D
Class Number(s) : VL2025260107270, VL2025260107262, VL2025260107310 VL2025260107260
Date of Examination : 7 October 2025, 9:30 – 11:00 am
Exam Duration : **90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M- Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply,4 – Analyse,5 – Evaluate,6 – Create)
- Course Outcomes :
  CO2 - To analyze and design sequential circuits utilizing various types of flip-flops
  CO3 - To analyze different instruction formats, addressing modes and validate efficient algorithms for fixed-point arithmetic operations

Q. No	Question	Marks	CO	BL
1.	In a process control unit 4-bit parallel data is being processed which needed to be converted in serial data for successful transmission. Design a 4-bit Parallel in Serial out (PISO) shift register to execute the conversion. Draw the circuit diagram and explain the working principle with taking an arbitrary binary input sequence 1010.	10	2	4
2.	In an embedded system any random value (0 to 7) is being assigned and then the value outcomes are expected to go down to lower values. Design an appropriate down counter by using T flip-flops.	10	2	6
3.	a) Discuss how the Harvard architecture achieves more robust and efficient outcomes compared to the Von Neumann architecture. Illustrate your explanation with their design differences and practical implications.	5	3	3
	b) Find the multiplication result of -6 × -7 by using Booth's algorithm.	5		
4.	a) Explain the execution process of a 2-address instruction set, highlighting the coordination between the CPU and memory. Support your explanation with a suitable example and an appropriate block diagram illustrating the data flow.	5	3	4
	b) Explain the concept of addressing modes and discuss their significance in the design of instruction sets. Compare and contrast at least four different addressing modes with examples, and analyze how the choice of addressing mode impacts instruction Performance.	5		

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5.	By using Restoring Division algorithm, find out the quotient and remainder for dividend = $(10)_{10}$ and divisor = $(3)_{10}$. Mention the flow chart (restoring division algorithm) and demonstrate the process with detailed steps and associated values.	10	3	5

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