VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SLOT: D1+TD1

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

Programme Name & Branch	**: B.Tech & CSE**
Course Code and Course Name	**: BACSE103 and Computation Structures**
Faculty Name(s)	**: Dr.S.Gayathri/Manoharan A/ Dr.Vani Rajasekar/ Mr. Soumyajyoti Dey/ Dr.R.Banupriya/ Dr.R.Prabhu/ Dr. Sultan Mahmood Chowdhury/ R.Hariprasad/ B.Priyadharshini / Dr.Prabin Jose J/ Dr. Satyajit Mohanty/ Dr.P.Gopinath/Dr. Muchenedi Hari Kishor**
Class Number(s)	**: 7232/7311/7302/7253/7251/7244/7249/7245 / 7241/7234/7304/7238/7240**
Date of Examination	**:08.10.2025**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)

  2. To analyze and design sequential circuits utilizing various types of flip-flops.
  3. To analyze different instruction formats, addressing modes and validate efficient algorithms for fixed-point arithmetic operations

Q. No	Question	Module	Marks	CO	BL
1.	A digital designer is working on a communication module that receives a 4-bit data stream (1, 0, 1, 1) from a sensor — one bit at a time, synchronized with a clock pulse. Two different circuit designs are tested for handling the incoming bits. Design A passes each single bit input to the next circuit stage immediately after every clock pulse. Design B takes single bit input on every clock pulse and then provides the complete 4-bit data (1, 0, 1, 1) simultaneously to a microcontroller for processing. Task: 1. Design a register for circuit A that provides a time-delayed serial output? 2. Design a register for circuit B that performs parallel output data conversion?	2	10	2	3
2.	A traffic light controller requires a digital circuit that cycles through eight timing states repeatedly, corresponding to binary counts from 000 to 111, and then resets to 000. The design must ensure that all flip-flops are triggered simultaneously by a common clock pulse. Derive the Boolean expressions for the D inputs of each flip-flop using the excitation table. Simplify the expression using K map and design a suitable counter to control the traffic light sequence.	2	10	2	3

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3.	A computer architect is designing the instruction set for a new processor. To evaluate the efficiency of different instruction formats, the following arithmetic operation is considered: **A = (B+C) * D** The goal is to implement this expression efficiently using different instruction formats supported by the processor depending on number of operands. Write the sequence of instructions required to execute the above expression using 3 address instructions, 2 address instructions, 1 address instructions and Zero address instructions.	3	10	3	3
4	An electronics engineer is designing a 4-bit unsigned multiplier for a small processor. To speed up multiplication, the engineer decides to implement a hardware algorithm that reduces the number of addition operations by analysing bit patterns in the multiplier. The numbers to multiply are: Multiplier (M) = 0101 (decimal 5) and Multiplicand (Q) = 0010 (decimal 2) Task: 1. Carry out the multiplication using a hardware-friendly algorithm that minimizes additions by interpreting the multiplier's binary patterns 2. Carry out the multiplication which further reduces the number of partial additions by grouping the multiplier bits in pairs using Booth recoding table	3	10	3	3
5	a) A microprocessor is executing a program stored in memory. The processor follows a standard four phases instruction cycle. The processor needs to perform the following instruction: **ADD R1, A, B** (Add the content of A and B, Store the result in R1) Describe step-by-step approach happens during each phase of the instruction cycle for this instruction.	3	5	3	2
	b) A processor is executing instructions to load data from memory into a register. In one method, the processor treats the source variable in the instruction as the exact memory location of the data. In another method, the processor treats the source variable in the instruction as the address of another memory location that contains the actual data. Explain these two addressing modes and compare their advantages.	3	5	3	2