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VIT
Vellore Institute of Technology

Reg. No:

Course: BACSE103 - Computation Structures

Final Assessment Test – November 2025

Class NBR(s): 7257/7259/7261/7263/7265/7269/7309

Time: Three Hours

Slot: C1+TC1

Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

COs	CO Statements
CO1	To design and optimize minimal combinational circuits.
CO2	To analyze and design sequential circuits utilizing various types of flip-flops.
CO3	To analyze different instruction formats, addressing modes and validate efficient algorithms for fixed-point arithmetic operations.
CO4	To understand the concept of memory organization and I/O fundamentals.
CO5	To understand the microcontroller architectural designs and parallel computing systems.

BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Answer ALL Questions

(10 X 10 = 100 Marks)

1. a) Convert the following hexadecimal $(DEAD.23F)_{16}$ into its equivalent decimal and octal representations. [5] CO1 BL4

   b) Design a Full Adder using two Half Adders. Derive the equations for Sum and Carry and draw the logic diagram. [5]

2.a) A process is allocated 3 cache blocks in memory. The reference string given is CO4 BL4

7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2

(i) Apply the FIFO cache replacement algorithm and show the contents of the cache after each reference. Calculate the total number of cache hits and misses.

(ii) Apply the LRU cache replacement algorithm for the same reference string and show the cache contents. Calculate the total number of cache hits and misses.

(iii) Compare and state which algorithm performs better for the given sequence.

OR

2.b) A computer system has a main memory of 64 KB and a cache of 1 KB with a block size of 16 bytes. CO4 BL4

(i) Explain how a memory address is divided into tag, block, and word fields for the following cache mapping policies: Direct Mapping, Fully Associative Mapping, Set-Associative Mapping (2-way).

(ii) For a memory address of 0x1A3F, show how the fields (tag, block/set, word) are identified under each mapping policy.

3. a) Insert the binary number 1001 into a 4-bit shift register using the Parallel-In Serial-Out (PISO) mode. Draw the logic diagram of a PISO register. Also, indicate how many clock cycles are required for loading the data and how many clock cycles are required for reading the data. [5] CO2

   b) Explain the race-around condition occurs in a JK flip flop and describe how the Master-Slave configuration eliminates this problem. [5]

4. Explain the concept of Instruction Level Parallelism (ILP) and Thread Level Parallelism (TLP) with an example showing how multiple threads can be executed in parallel. Illustrate both ILP and TLP with neat diagrams. CO5

5. a) Write an ARM assembly program to add three numbers 5, 10, and 15, using the immediate addressing mode. Store the result in register R0 and explain the instructions used? [5] CO5

   b) Compare and contrast a microprocessor and a microcontroller. [5]

6. Using the Non-Restoring Division Algorithm, perform the division of 13 by 3. where 13 is Dividend and 3 is Divisor. CO3

   Draw the algorithm/flowchart for the Non-Restoring Division process and show the step-by-step execution.

7. From the given arithmetic expression, write an assembly language program using (zero, one, two, three) address instruction formats. CO3

$$a = x - y$$
$$b = a - x$$
$$c = b - a$$
$$d = a^{-1}$$

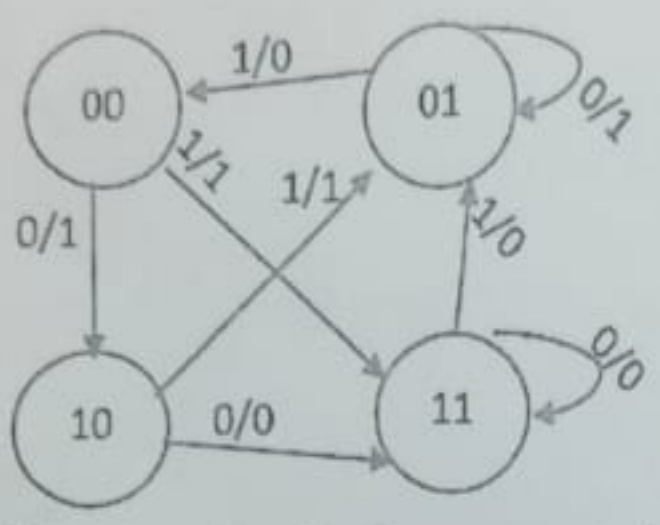
   Show the contents of the accumulator (AC) and registers after each computation in every instruction. Explain the final output for each instruction formats if the value of x=5 and y =13.

8. a) Draw and explain the basic working of a DMA controller. [5] CO4

   b) In a computer system, data transfer between the CPU and I/O devices is carried out using Programmed I/O, which results in low CPU utilization and reduced system efficiency. Suggest any two alternative methods that can overcome this limitation and explain how each method improves overall system performance. [5]

9. Explain the concept of a multiplexer and describe where it is used. Consider a multiplexer with four data inputs and determine how many select lines are required for its operation. Identify the type of this multiplexer then Construct the truth table for the 4-input multiplexer and write the Boolean equation that relates its output to the inputs and select lines. Also, implement the Boolean function $F(A, m, n) = \sum(2,3,4,6)$ using a multiplexer and derive the Boolean expression for the function using the multiplexer. CO

10.a)



A and B represent the flip-flop states, x is the input, and y is the output. The given state diagram consists of four states labeled 00, 01, 10, and 11, with each transition marked as input/output. Construct the corresponding state table showing the present states, next states, and output values for all possible input conditions. Using this state table, derive the state equations for A and B (next-state functions) and the output equation for y. Based on these equations, draw the circuit using D flip-flops along with the required combinational logic. Finally, determine whether the given state diagram represents a Mealy or Moore finite state machine (FSM), and explain the key characteristics and operational differences of that FSM type with reference to the given system.

OR

10.b) Design and implement a synchronous MOD-10 (decade) down counter using four T flip-flops. **CO2**

i. Draw the state diagram and state transition table showing present state and next state for decimal 0 to 9.

ii. Derive the Boolean expressions for the T inputs as minimized functions. Show the K-map groupings clearly and indicate the don't-care states used.

iii. Draw the logic diagram of the counter showing the T inputs implemented with basic logic gates and four T flip-flops.

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