V/D/TY

Reg. No: 23BIT0428

VIT
Vellore Institute of Technology

Final Assessment Test – April 2025

Course: BITE301L - Computer Architecture and Organization
Class NBR(s): 2704/2719/2725
Slot: A2+TA2
Time: Three Hours
Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

Answer ALL Questions
(10 X 10 = 100 Marks)

1.(a) Consider two different machines, with two different instruction sets, both of which have a clock rate of 200MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

Instruction Type	Machine A Instruction Count (Millions)	Machine A Cycles per Instruction	Machine B Instruction Count (Millions)	Machine B Cycles per Instruction
Arithmetic and logic	8	1	10	1
Load and store	4	3	8	2
Branch	2	4	2	4
Others	4	3	4	3

i) Determine the effective CPI, MIPS rate and execution time for each machine.
ii) Comment on the results

OR

1.(b) i) Determine the steps needed to execute the machine instruction [6]

Sub R1, R2, R3

in terms of transfers between the components the processor and the memory. Assume that the instruction itself is stored in the memory at location INSTR and that this address is initially in register PC.

ii) Explicate with neat sketch on how the operating system overlaps processing, disk transfers, and printing for several programs to make the best possible use of the resources available. [4]

2. Let us consider the assembly language program given below. The program consists of 10 instructions. Assume Register R2 contains 100 and Program counter contains 350.

```
LOAD 100
ADD (200)
SUB 300
MUL #3
STORE R1
LOAD (R1)
SUB –(R1)
ADD (R1)+
SUB 100(R1,R2)
ADD 200(PC)
```

Address	Value
99	100
100	200
101	300
200	400
299	650
300	800
301	750
500	600
400	700
550	250
800	900
802	950

Execute the program and identify the following information for each instruction using the values which are given in the table: **(Note: Each instruction depends on each other).**

a) Type of the addressing mode used

b) Effective address

c) Content of the registers (Accumulator and R1) after the execution of each instruction

Instruction	Type of the addressing mode used	Effective address	Content of the Accumulator register after the execution	Content of the R1 register after the execution

3) Write a program to evaluate the arithmetic statement:

$$Y = \frac{(M * N) + O}{P - Q}$$

a) Using an accumulator type computer with one address instruction.

b) Using a stack organized computer with zero-address instructions

c) Using a general register computer with two address instructions

d) Using a general register computer with three address instructions.

Where M, N, ... Q and Y are memory addresses. In accordance with programming language practice, computing the expression should not change the value of its operands.

4. Let us consider the situation where a number of devices capable of initiating interrupts are connected to the processor. Because these devices are operationally independent, there is no definite order in which they will generate interrupts. For example, device X may request an interrupt while an interrupt caused by device Y is being serviced, or several devices may request interrupts at exactly the same time. Answer the following questions:

a) How can the processor recognize the device requesting an interrupt?

b) Given that different devices are likely to require different interrupt-service routines, how can the processor obtain the starting address of the appropriate routine in each case?

c) Should a device be allowed to interrupt the processor while another interrupt is being serviced?

d) How should two or more simultaneous interrupt requests be handled?

5. A computer employs RAM chips of 128 x 8 and ROM chips of 512 x 8. The computer system needs 256 x 8 of RAM, 1024 x 16 of ROM, and two interface units with 256 registers each. Each register size is 8-bits. A memory mapped I/O configuration is used.

a) Compute the following requirements.

S.No.	Memory	N x W	$N^1 \times W^1$	p	q	p * q	x	y	z	Total

b) Compute total number of decoders are needed for the above system?

c) Design a memory-address map for the above system.

d) Show the chip layout for the above design.

6. Consider a system with paging-based memory management whose architecture allows for a 16MB virtual address space for processes. The size of logical page and physical frame is 2MB. The system has 8MB of physical RAM. A process is divided into 8 pages numbered 0–7. The processor accesses pages in the following sequence:

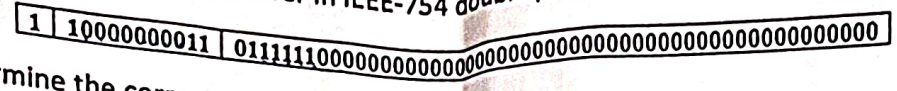
3, 4, 5, 3, 2, 1, 4, 5, 2, 3, 1, 4, 5, 3, 2, 1, 3, 4, 5, 1.

Identify the number of frames in the physical memory. Assume that the RAM is initially empty and that there is no other process executing on the system. Calculate the number of page faults generated and hit ratio and miss ratio for the following replacement algorithms.

a) FIFO page replacement algorithm.
b) LRU page replacement algorithm.
c) Optimal page replacement algorithm.

Identify what would be the lowest number of page faults achievable in this case?

7. a) Consider the following number in IEEE-754 double precision representation: [5]



Determine the corresponding decimal number.

b) Perform the arithmetic operations given below with binary numbers and with negative numbers in signed-2's complement representation. Use seven bits to accommodate each number together with its sign. In each case, determine if there is an overflow. [5]

(i) (–25) + (–38) (ii) (–25) - (–38)

8.(a) Construct the flow chart and display the step-by-step multiplication process of Booth algorithm when subsequent numbers are multiplied.

Multiplicand = 63
Multiplier = -17

Show the contents of the registers AC and QR and SC during the multiplication process. Use 7-bit register to accommodate the value.

OR

8.(b) Construct the flow chart and display the step-by-step division process for unsigned non-restoring division method. Perform the division operation with binary numbers using non restoring method.

25 ÷ 10

Show the contents of the register A, Q & SC during the division process.

9. a) A non-pipelined single cycle processor operating at 300 MHz is converted into a synchronous pipelined processor with five stages requiring 1.5ns, 1ns, 2.5ns, 3.5ns and 2ns respectively. The delay of the latches is 1.0 ns. Calculate the cycle time and speedup of the pipeline processor. [5]

b) A five-stage pipeline has the stage delays as 200, 250, 130,110 and 100ns respectively. Registers are used between the stages and have a delay of 10ns each. Identify the cycle time and total time taken to process 2000 data items on the pipeline. [5]

10. Illustrate the concept of array processor in detail.

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