Y/D/TY

Reg. No:

VIT
Vellore Institute of Technology

Final Assessment Test – April 2025

Course: BCSE205L - Computer Architecture and Organization

Class NBR(s): 1363/1365/1379/1382/1386/1389/ 1393/1395/1403/1417/1419/1421/1423/1425/1427/ 1431/1435/1441/1445/1449/1454/1476

Slot: C1+TC1

Time: Three Hours

Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Perform an assembly language code and register transfer notation to evaluate the following arithmetic expression using IAS instructions.

$$S = (A - (B+C)) \times (D - (E+F))$$

Assume that data variables A, B, C, D, E, F are available at memory locations 200, 201, 202, 203, 204, 205 respectively. And S will be stored 500 onwards.

2. Illustrate Non- Restoring division algorithm and apply the same to divide the dividend 23 by the divisor 5. Show how the q_0 bit is replaced in each iteration.

3. i. Consider the expression **T = P + (Q – R) × S** and assume that data will occupy 24 bits, address occupy 24 bits and word length is 1 byte. **[6]**

   a) Evaluate the above expression for 3 address and 2 address machines.
   b) Calculate the memory to store and encode each of these sets in bytes.
   c) Calculate memory traffic in terms of memory accesses to fetch and execute the instruction.

   ii. Assume two different processors A and B executes the same instruction set with clock rate 5GHz and 6GHz respectively. The cycles per instruction of A is 2.0 and B is 3.5. Which processor among A and B performs best in terms of instructions per second? **[4]**

4. A computer employs RAM chips of 256 × 8 and ROM chips of 128 × 8. Design a computer system that needs 256 x 16 of RAM, 256 x 8 of ROM, and two interface units with 256 registers each. A memory mapped I/O configuration is used. The two higher -order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.

   a) How many chips are needed in total for the design?
   b) Design a memory interface address map for the above system.
   c) Show the chip layout for the above design.

5. Explain how DMA transfers data to and from the peripherals with necessary sketch and Illustrate the different data transfer methods in DMA.

6. Delineate disk stripping? Illustrate the RAID levels that uses different types of stripping. Discuss their advantages and disadvantages.

7. i. Elaborate on Flynn's Taxonomy that involves multiple instructions. Highlight the role of shared and distributed memory in parallel machines. [6]

ii. Differentiate super pipeline architecture from scalar pipeline architecture? [4]

8. Consider the following sequence of instruction in a 4-stage (F, D, E, W) pipelined execution. Sketch the space - time diagram. Identify the hazard that occurs while executing the instructions and explain the techniques to overcome this hazard.

MOV A, B [A <-B]
ADD C, B, A [C <- A + B]
SUB C, #5 [C<- C – 5]

9.a) i. Apply bit-pair recoding table for booth multiplication to find the recoded multiplier bits of 13 and use the recoded multiplier bits to multiply 31 × 13. [5]

ii. Apply Booth Multiplication and show how it works efficiently to multiply 18 and -8. [5]

OR

9.b) i. With a neat sketch, explain the IEEE-754 standard floating point formats. Represent 6784.234_{10} in single precision and double precision format. [6]

ii. Explain the steps involved in performing floating point multiplication and division. [4]

10.a) Consider a cache of 128 blocks of 256 words each and a byte addressable main memory consisting of 16,384 blocks.

i. Calculate the number of bits required to address a main memory block.
ii. Find the split of the physical address bits assuming the cache is direct, fully associative and 4-way set associative mapped.
iii. Analyse the impact of using these mapping techniques for the above scenario.

OR

10.b) i. Consider the following sequence of memory references. 4, 0, 4, 2, 1, 6, 2, 5, 0, 5, 1, 7, 6, 2, 3. [8]

Calculate hit ratio and miss ratio using FIFO and LRU with 4 cache lines.

ii. Consider a computer system that employs a cache with an access time of 45 ns and a main memory with a cycle time of 550 ns. Suppose that the hit ratio for reads is 75%, what would be the average access time for reads if the cache is a "look-Aside" cache? [2]

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