VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SCHOOL OF COMPUTER SCIENCE ENGINEERING AND INFORMATION SYSTEMS
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026

SLOT: G1

Programme Name & Branch	: B.Tech [IT]
Course Code and Course Name	: BITE301 – COMPUTER ARCHITECTURE AND ORGANIZATION
Faculty Name(s)	: Prof. Sumathy.S, Prof. Sumathi.D, Prof. Raghavan R, Prof. N.Krishnamoorthy
Class Number(s)	: VL2025260502758, VL2025260502756, VL2025260502754, VL2025260502751
Date of Examination	: 02.02.2026
Exam Duration	: **90 minutes**

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)

1.. Elucidate the arithmetic operations, addressing modes and the performance of Computers.

2. Design instruction level parallelism using instruction stages. Understand pipelining concepts and identify the hazards to rectify in typical processer pipeline.

Q. No	Question	M	CO	BL
1.	a) Consider a 3.6 GHz CPU, where executing data processing instructions takes 8 clock cycles and executing data transfer instructions takes 10 clock cycles. When a specific program of one million instructions run, 60% of the instructions are data processing and 40% of the instructions are data transfer. Compute the total execution time for the program.	5	CO1	2
	b) A CPU is driven by 4 GHz clock. Compute the duration of one clock cycle. Assume that on average the execution of an instruction takes 8 clock cycles. Compute the performance of the CPU in terms of MIPS. If executing a specific program of 200 million instructions takes 2 seconds, how many clock cycles it would take on average to execute an instruction of the program.	5		
2.	a) Match the following			

i	Memory Address Register (MAR)	Contains the address of the next instruction to be executed
ii	Memory Data Register (MDR)	Intermediate arithmetic and logic operation results are stored
iii	Accumulator (AC)	Contains the current instruction during processing
iv	Program Counter (PC)	Holds the memory location of data that needs to be accessed
v	Instruction Register (IR)	Holds data that is being transferred to or from memory

	5	CO2	2

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	b) A 6 stage (k) pipeline requires 60 ns (t_p) for each stage of the pipeline to perform a sub-operation. Determine the execution time for 300 tasks (n) in a **pipelined system and a non-pipelined system** and specify the **speedup** and **efficiency** achieved.	5			
3.	a) Perform the arithmetic operations with the given data in signed- 2's complement representation. Use eight bits to accommodate each number together with its sign. Determine if there is an overflow by checking its carry into and out of sign bit position. i) (-35) + (-40) ii) (+35) + (-40) iii) (-35) - (+40) iv) (-35) - (-40)	8	CO1	2	
	b) The following binary word W = 1100 0101 1101 0010 is stored in a 16 bit register. What is the **decimal number** represented by W if the given binary word is interpreted as an integer in each of the following codes: a) sign-magnitude; b) two's complement number.	2			
4.	Evaluate the following arithmetic expression on writing the sequence of instructions, • Using a general register computer with **three address** instructions. • Using a general register computer with **two address** instructions. • Using an accumulator type computer with **one address** instructions. • Using a stack organized computer with **zero-address** operation instructions. $Y = (A*B)/(C-(D+E))$, where A, B, C, D and E are memory addresses. In accordance with programming language practice, computing the expression should not change the original value of its operands.	10	CO2	3	
5.	Registers R1 and R2 of a computer contains the decimal values 4500 and 5600. Base Register BX contains 1500 and index register XR contains 2000. Identify the effective address of the memory operand and type of addressing mode of each of the following instructions. i) Move #6700, R4 ii) Store R6, 60 [BX, XR] iii) Load AC, 500 [XR] iv) Add -(R2) , R5 v) Mov R1, [BX] 24 vi) Mov R2, [XR] [BX] vii) Store R5, 2400 viii) Load [2400], R5 ix) Add R1, R2, R3 x) Sub (R1)+, R6	10	CO1		