REG.NO.:

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2024-2025

SLOT: E1

Programme Name & Branch :B.TECH Electronics Engineering (VLSI Design and Technology)
Course Code and Course Name : BEVD207L and Computer Architecture
Faculty Name(s) : JAYAKRISHNAN P
Class Number(s) : VL2024250500780
Date of Examination : 31/01/2025
Exam Duration : 90 minutes **Maximum Marks: 50**

General instruction(s): Answer All Questions

Q. No	Question	M	CO	BL
1.	Assuming the following address and register contents, A has value 5. Determine the content of Accumulator after execution of instruction MOV A, (mode)3 If following Addressing modes are used i. Register Addressing (consider R3) ii. Register indirect (consider R3) iii. Immediate iv. Direct v. Indirect List down the effective address and content of Accumulator using.	10	4	3
2.	What are the different instruction formats in RISC-V 32I processor? Give the bit division of any three-instruction format.	10	4	4
3.	a) Perform Multiplication of -11× -10 using Booth's algorithm.	7	2	3
	b) Use 2's complement arithmetic to perform the subtraction of $17_{16} - 2A_{16}$	3		
4.	Programs P1 and P2 have been run on two machines M1 and M2. The execution times have been recorded in Table 1. Which machine is faster for each program and by how much (relative)? Table 1 (i) Calculate the execution rate (instruction per second) for each machine running program P1, when P1 requires execution of 300 million instructions on machine M1 and 180 million instructions on machine M2. (ii) Given that the clock rates for machines M1 and M2 are 200MHz and 300MHz respectively, determine the clock cycles per instruction for program P1 on each machine.	10	1	3
5.	Discuss Von-Neumann architecture of a computer with an example	10	1	2

Address					Register				
Location	1	2	3	4	5	1	2	3	4	5
Content	4	2	1	6	5	4	5	4	3	2

Program	Time on M1	Time on M2
P1	5 Seconds	15 Seconds
P2	2 Seconds	4 Seconds

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