School of Computer Science Engineering and Information Systems
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2024-2025

SLOT: A2 + TA2

Programme Name & Branch : **BTECH IT**
Course Code and Course Name : **Computer Architecture and Organization & BITE301L**
Faculty Name(s) : **Dr. M.Angulakshmi, Dr. M. Vanitha, Dr. S.Meenatchi**
Class Number(s) : **VL2024250502704,VL2024250502725,VL2024250502719**
Date of Examination : **16-Mar-2025**
Exam Duration : **90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (2 – Understand, 3 – Apply)
  - CO3- Analyse the arithmetic algorithms to perform ALU operations
  - CO4- Design a memory system on understanding the chip organization and analyse its performance

Q. No	Question	M	CO	BL
1	a. Demonstrate the step-by-step multiplication process using sign magnitude multiplication algorithm when the following numbers are multiplied. A = + 37 (Multiplicand) B = -35 (Multiplier).	6	3	3
	b. Perform signed magnitude addition and subtraction for the values a. (+ 8) + (- 6) b. (+8) - (-6)	4		
2.	Divide the following positive numbers using the non-restoring division algorithm. Assume Dividend as 57 and the Divisor as 13.	10	3	3
3.	A computer employs RAM chips of 1024 x 8 and ROM chips of 1024 x 4. The computer system needs 2K*16 bytes of RAM, and 1K *8 bytes of ROM and two interface units of 512 register each.		4	3
	a. Draw the memory address map for the system.	4		
	b. How many lines must be decoded for chip select?	3		
	c. Draw the memory chip connection diagram.	3		
4.	a. Consider a Direct mapped cache of size 32 KB with block size 512 bytes. The size of main memory is 256 KB. Find- Number of bits in Tag and Tag directory size.	3	4	3
	b. Consider a Fully associative mapped cache of size 512 KB with block size of 4 KB. There are 10 bits in the tag. Find the Size of main memory.	3		
	c. A 4-way Set Associative cache memory consists of 128 lines. The main memory consists of 16,384 blocks and each block contains 256 bytes. How	4		

REG.NO.:

VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act 1956)

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	many bits are required for addressing the main memory? How many bits are needed to represent the TAG, SET and BLOCK Size fields?			
5.	Given Page reference string 7, 6 , 3 , 2 , 3, 4, 5, 3, 2, 6, 7, 3, 2, 4, 5, 7, 2, 4,1, 6, 7, 6 ,3, 2, 3, 4, 5, 3. How many page faults would occur for the following replacement algorithms, assuming 5 frames (initially empty). Also Calculate Hit ratio, Miss ratio for each method given below. a. FIFO b. LRU c. Optimal	 3 3 4	4	2

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