REG.NO.:

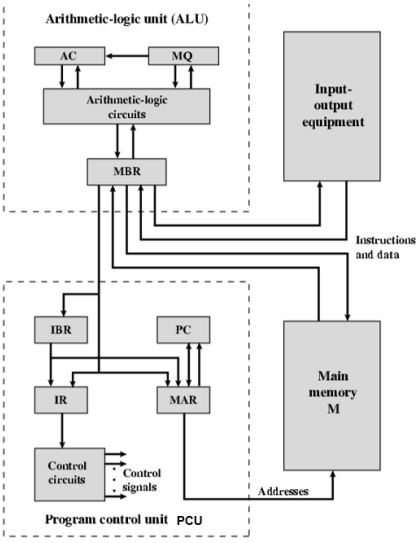
SLOT: A1 +TA1

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026

Programme Name & Branch	**: BCE, BAI, BCB, BCI, BCT, BCT, BDS, BKT, BME, BEL, BYB**
Course Code and Course Name	**: BCSE205L and Computer Architecture and Organization**
Faculty Name(s)	**: Common to all classes**
Class Number(s)	**: VL2025260501998, 1988, 1903, 2001, 1866, 1985, 1870, 1953, 1898, 4005, 1901, 2024, 5391, 1880, 3865, 1896, 2022, 2006, 1968, 1873**
Date of Examination	**: 27/01/2026**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes:
  CO1: Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating point arithmetic operations.

Q. No	Question	Modu
1.	Explain the architecture of the IAS computer with the help of a neat block diagram. Using the instruction sequence, X=A/B, illustrate the flow of data and control information through the IAS registers during the execution of this instruction sequence. ANS: (5 marks) ▪ **MBR: Memory Buffer Register** - contains the word to be stored in memory or just received from memory. ▪ **MAR: Memory Address Register** - specifies the address in memory of the word to be stored or retrieved. ▪ **IR: Instruction Register** - contains the 8-bit opcode currently being executed. ▪ **IBR: Instruction Buffer Register** - temporary store for RHS instruction from word in memory. ▪ **PC: Program Counter** - address of next instruction-pair to fetch from memory. ▪ **AC: Accumulator & MQ: Multiplier quotient** - holds operands and results of ALU ops.  Instruction Sequence: (5 marks) LOAD M(A), DIV M(B)	1

STOR M(X), LOAD MQ
STOR M(X)

LOAD M(A), DIV M(B)

MAR ← PC

MBR ← M[MAR]

IBR ← MBR<20…39>

IR ← MBR<0…7>

MAR ← MBR<8…19>

MBR ← M[MAR]

AC ← MBR
IR ← IBR<0..7>

MAR ← IBR<8..19>

MBR ← M[MAR]

AC, MQ ← AC ÷ MBR

PC ← PC + 1

MBR ← AC

M[MAR] ← MBR

IR ← IBR<0…7>

MAR ← IBR<8…19>

PC ← PC + 1

STOR M(X), LOAD MQ
STOR M(X)

MAR ← PC

MBR ← M[MAR]

IBR ← MBR<20…39>

IR ← MBR<0…7>

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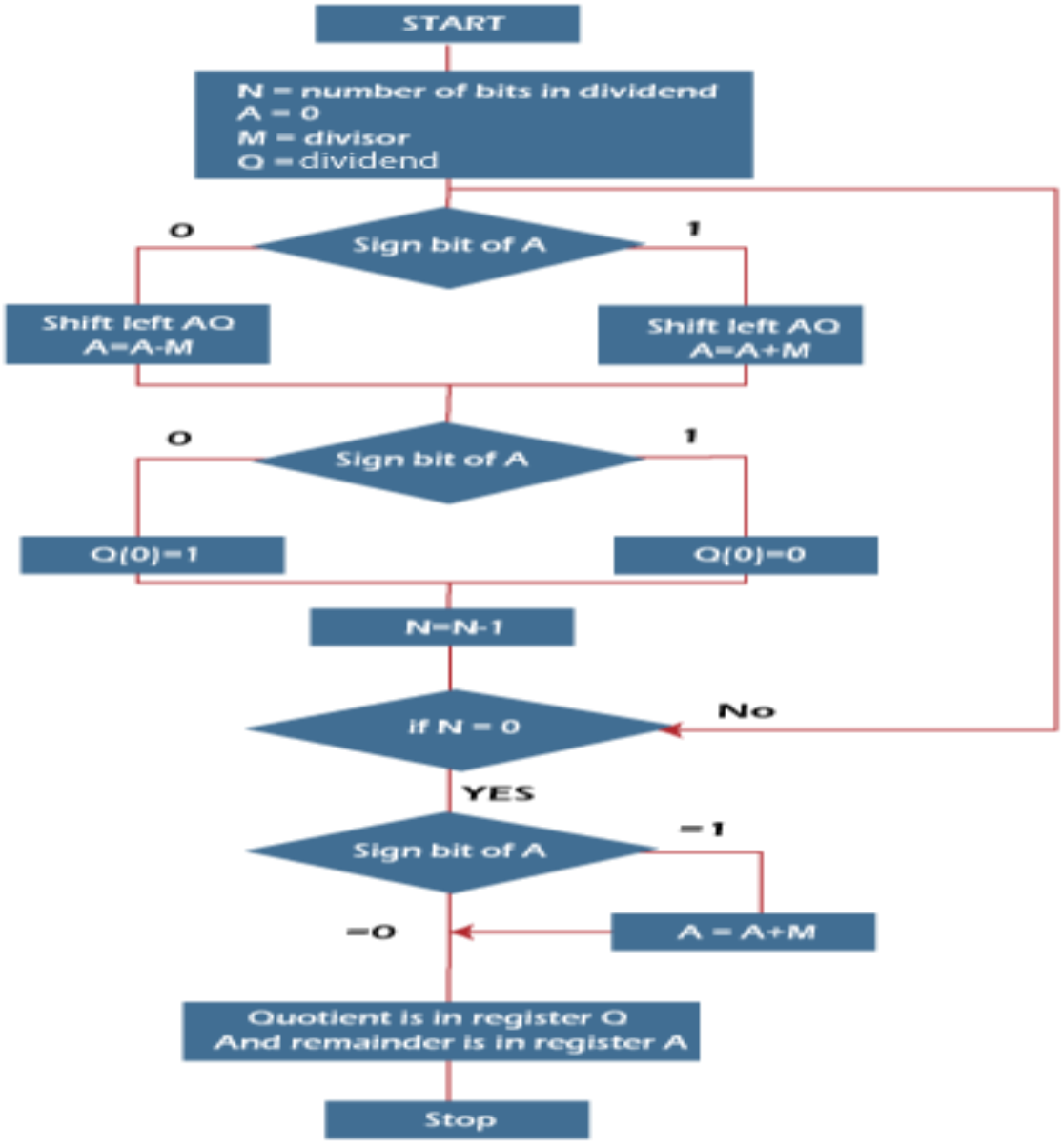
	MAR ← MBR<8…19> AC ← MQ	
2.	Apply the non-restoring division algorithm to divide 18 by 6, showing the contents of the accumulator and quotient register at each iteration. Explain the operational flow of the non-restoring division using a suitable flowchart. ANS: (4 marks)  Solution: 18/6 (6 marks)	2

n	M	A	Q	Operation
5	000110	000000	10010	initialize
5	000110	000001	0010_	shift left AQ
		111011	0010_	A=A-M
		111011	00100	Q[0]=0
4	000110	110110	0100_	shift left AQ
		111100	0100_	A=A+M
		111100	01000	Q[0]=0
3	000110	111000	1000_	shift left AQ
		111110	1000_	A=A+M
		111110	10000	Q[0]=0
2	000110	111101	0000_	shift left AQ
		000011	0000_	A=A+M
		000011	00001	Q[0]=1
1	000110	000110	0001_	shift left AQ
		000000	0001_	A=A-M
		000000	00011	Q[0]=1

register Q contain the quotient 3 and register A contain remainder 0

3.	a) Using Modified Booth's algorithm, find the product of –21 × 5. ANS: METHOD1	2

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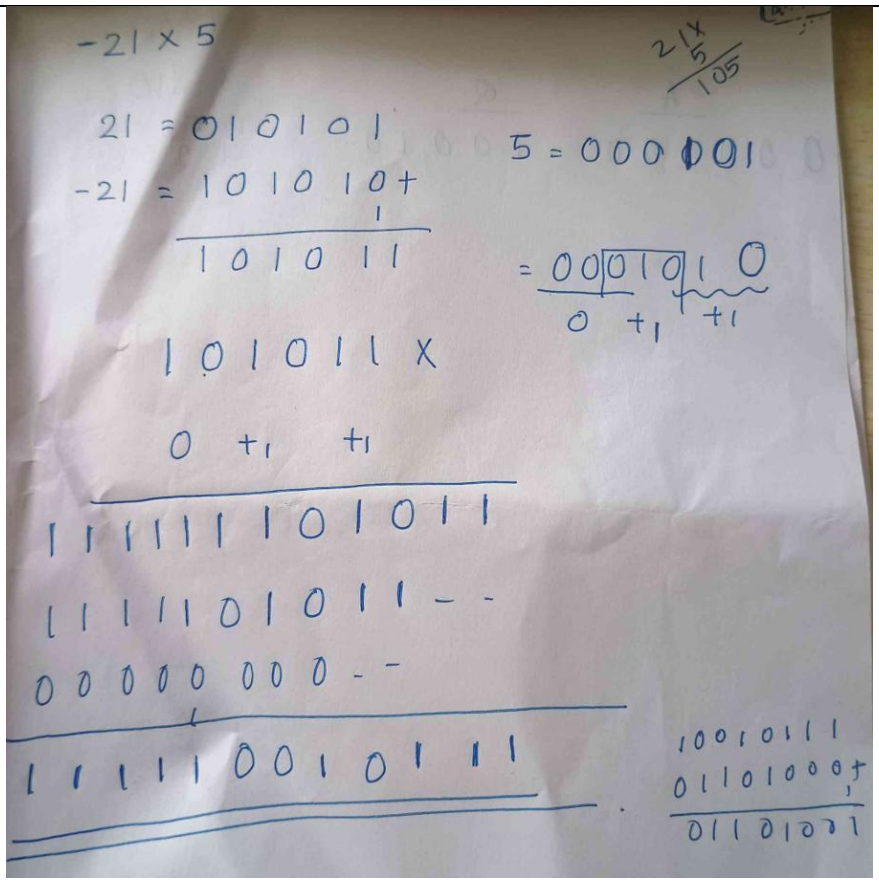
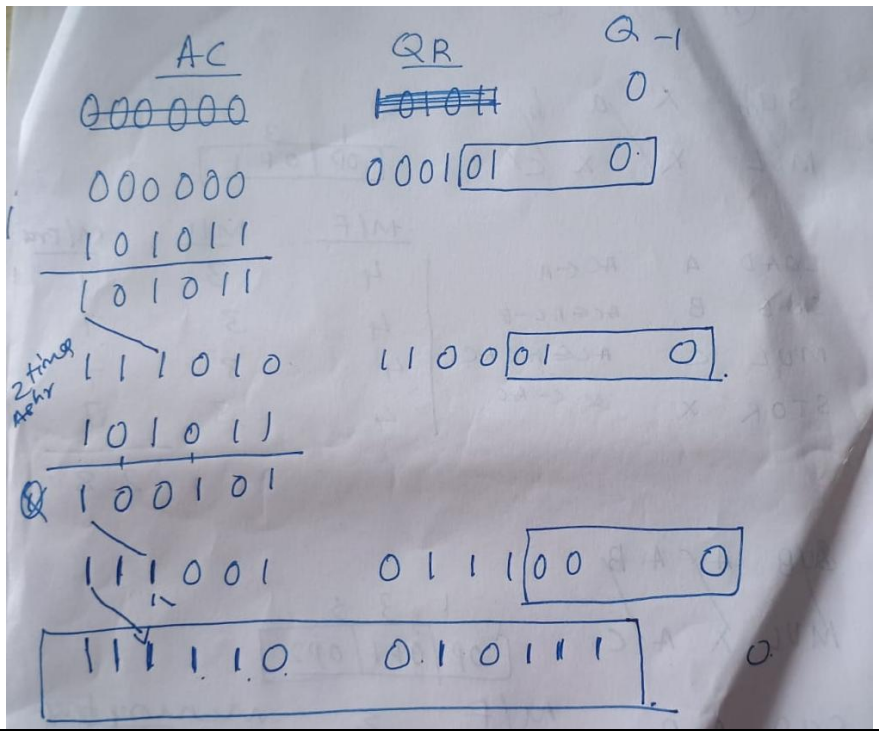


METHOD 2



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b) Highlight the advantages of Modified Booth's algorithm over conventional Booth multiplication — 2

ANS:

1. Faster multiplication (Modified booth processes 2 bits at a time. This reduces the number of partial products)
2. Reduced hardware
3. Lower power consumption

4. Consider a processor with the following initial system state: — 3
   - Instruction stored at memory location 300
   - Address field stored at location 301 with a value of 600
   - Index register R1 = 200

   a) Calculate the effective address for (4 marks)
   - Direct addressing mode
   - Indirect addressing mode
   - Auto increment addressing mode
   - Immediate addressing mode

   b) Analyze how relative addressing and indexed addressing compute the effective address using the given system state. (2 marks)

   c) Suppose the program is relocated and the instruction moves from memory location 300 to 1300. Recompute the effective address for both addressing modes. Evaluate the impact of program relocation on relative and indexed addressing mode and justify your answer. (4 marks)

ANS: a) & b)

Addressing mode	EA	Value
Direct addressing mode	600	
Indirect addressing mode	M[600]	
Auto increment addressing mode	200	
Immediate addressing mode	301	600
Relative addressing mode	EA=302+600=902	
Indexed addressing mode	EA=600+200=800	

d) After relocation

Relative addressing mode: EA = 1302 +600 = 1902

Indexed addressing mode: EA = 600 + 200 = 800 (remains unchanged – EA depends on register + address)

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5.

a) Compare RISC and CISC. 1

ANS:

RISC	CISC
It is a Reduced Instruction Set Computer.	It is a Complex Instruction Set Computer.
It focuses on Software.	It focuses on Hardware.
It uses only a Hardwired control unit.	It uses both hardwired and microprogrammed control units.
Transistors are used for more registers.	Transistors are used for storing complex instructions.
Code size is large.	Code size is small.
The uses of the pipeline are simple in RISC.	Uses of the pipeline are difficult in CISC.
An instruction is executed in a single clock cycle.	Instruction may take more than one clock cycle.
An instruction can fit in one word.	Instructions are larger than the size of one word.
The execution time of RISC is very short.	The execution time of CISC is longer.
The program written for RISC architecture needs to take more space in memory.	The Program written for CISC architecture tends to take less space in memory.

b) Assume a computer system in which both address and data fields are 24 bits wide, and the word length is 8 bits.

i) Analyze how the expression

$$X = (A - B) \times C$$

is evaluated using a one-address instruction format and a two-address instruction format. (2 mark) 3

ii) Determine the number of memory accesses (memory traffic) involved. (3 mark)

ANS:

ONE ADDRESS

Code	M/As to Fetch	M/As to Execute	Memory Traffic
LOAD A	4	3	4 + 3 = 7
SUB B	4	3	4 + 3 = 7
MUL C	4	3	4 + 3 = 7

STOR X	4	3	4 + 3 = 7
TOTAL			28

TWO ADDRESS

Code	M/As to Fetch	M/As to Execute	Memory Traffic
SUB A,B	7	9	7 + 9 = 16
MUL A,C	7	9	7 + 9 = 16
MOV X,A	7	9	7 + 9 = 16
TOTAL			48

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