REG.NO.:

SLOT: A2+TA2

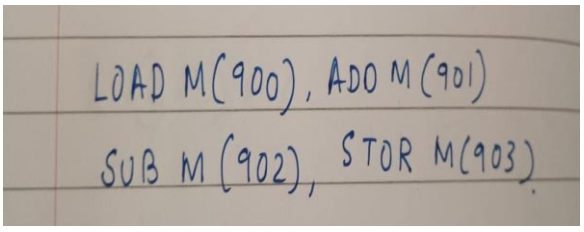
VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026

Programme Name & Branch : **B.Tech CSE**
Course Code and Course Name : **BCSE205L & Computer Architecture and Organization**
Faculty Name(s) : **Common to all**
Class Number(s) : **Common to all**
Date of Examination : **27.01.2026**
Exam Duration : **90 minutes** **Maximum Marks: 50**

General instruction(s):

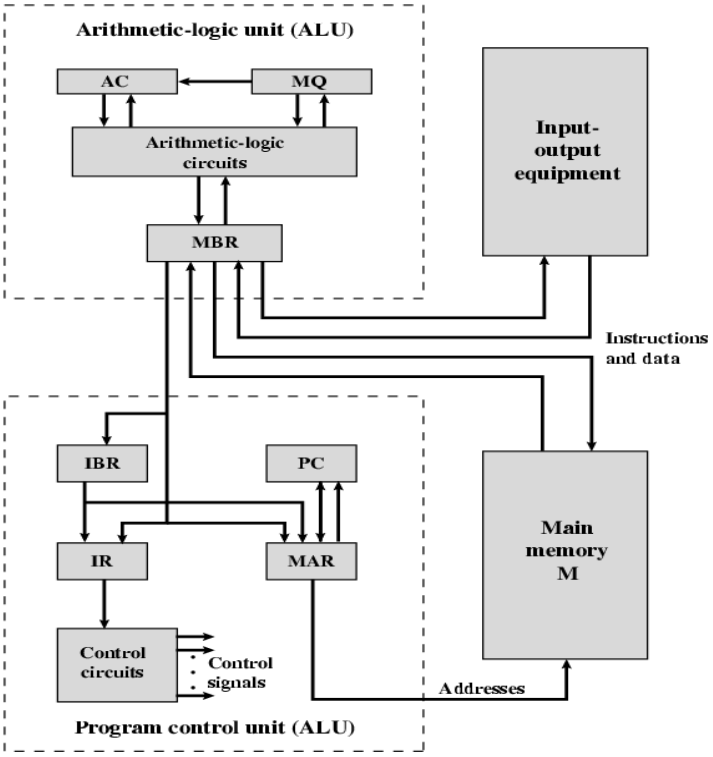
- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)
  CO1- Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating point arithmetic operations.

Q. No	Question	Module	Marks	CO	BL
1.	Consider the following expression using the IAS computer Instruction set and interpret the flow of the IAS computer architecture (Register flow of operations) with neat diagram. K = (M + N) – O Assume the memory locations 900, 901, and 902 for P, Q, and R respectively.  1. Instruction Fetch Cycle PC → MAR Memory → MBR MBR → IR / IBR PC ← PC + 1	1	7	1	BL 2

	2. Execute LOAD M(900) MAR ← 900 MBR ← M(900) AC ← MBR 3. Execute ADD M(901) MAR ← 901 MBR ← M(901) AC ← AC + MBR 4. Execute SUB M(902) MAR ← 902 MBR ← M(902) AC ← AC − MBR 5. Execute STOR M(903) MAR ← 903 MBR ← AC M(903) ← MBR Register Function PC Holds next instruction address MAR Holds memory address MBR Holds instruction/data from memory IR Holds current instruction IBR Holds next instruction AC Holds intermediate and final result				

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026

					
1b)	Compare and contrast Von Neumann and Harvard computer architectures. Ans: **Feature** / **Von Neumann Architecture** / **Harvard Architecture** Memory / Single memory for both instructions and data / Separate memory for instructions and data Buses / Single bus for instructions and data / Separate buses for instructions and data Instruction & Data Access / Cannot access both simultaneously / Can access both simultaneously Performance / Slower due to **Von Neumann bottleneck** / Faster due to parallel access Hardware Complexity / Simple design / More complex design	1	3		
2.	a) Perform 21/11 using Restoring division algorithm and explain the steps clearly and draw the flowchart. Give flowchart for the restoring division with combination of positive and negative numbers. (10)	2	10	1	BL 5

Step 1: Represent the numbers in binary

- Dividend $Q = 21_{10} = 10101_2$ (5 bits)
- Divisor $M = 11_{10} = 01011_2$ (5 bits)

We assume the **Accumulator (A)** is initialized to 0 and has enough bits to hold intermediate results.

Restoring Division Algorithm (Steps)

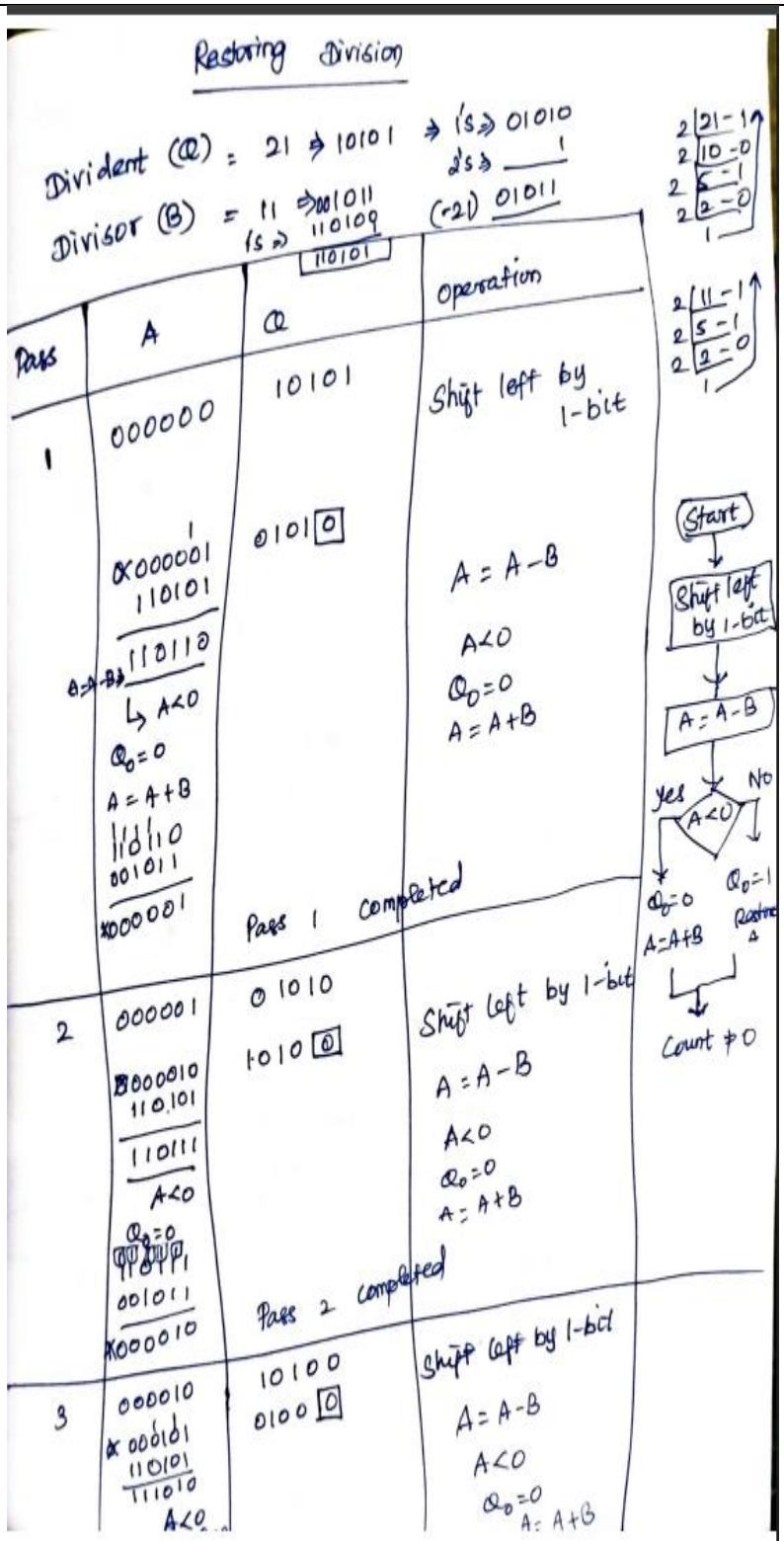
Registers:

- **A** = Accumulator (initialized to 0)
- **Q** = Dividend register
- **M** = Divisor register
- **n** = Number of bits in Q

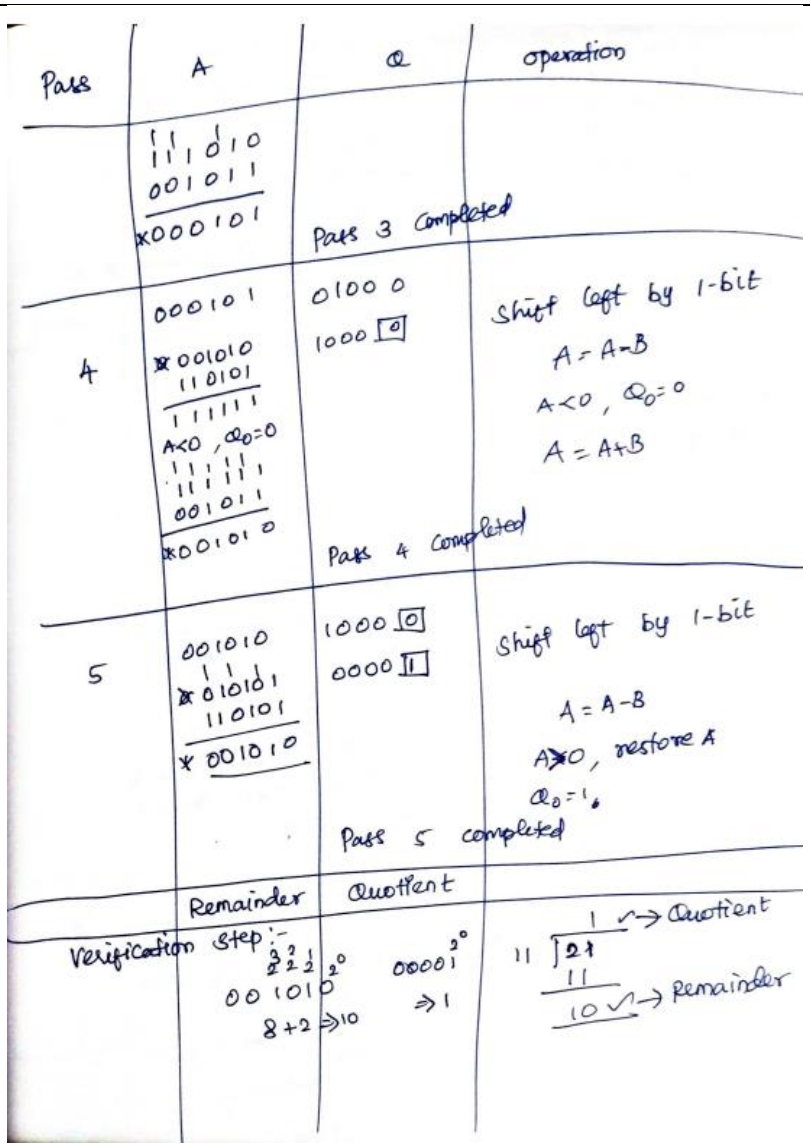
Algorithm Overview:

1. Initialize $A = 0$, $Q =$ Dividend
2. Repeat **n times**:
   - Shift **A and Q** left by 1 bit
   - Subtract divisor M from $A \rightarrow A = A - M$
   - If $A < 0$:
     - Restore $A = A + M$
     - Set **least significant bit of Q = 0**
   - Else:
     - Set **least significant bit of Q = 1**

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026



SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026

					
3.	a) Using Booth's algorithm, multiply (+12) × (−5) with neat flowchart based explanation.	2	7	1	BL 5

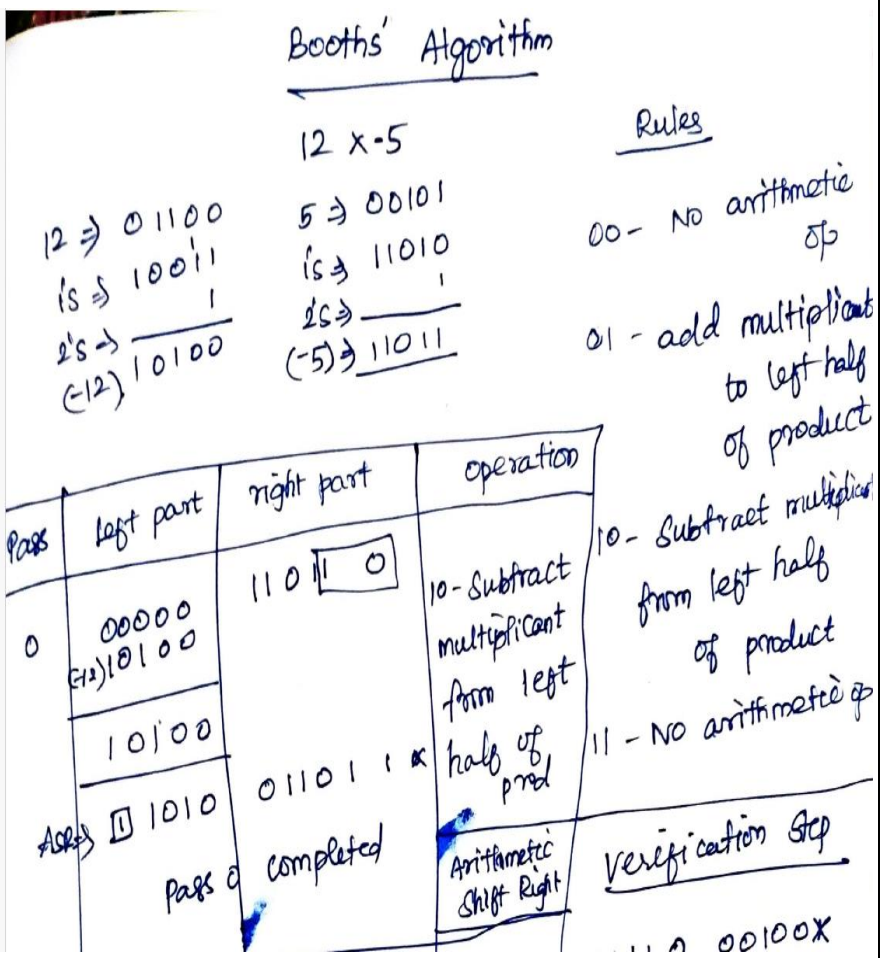
SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026

Step 1: Choose number of bits

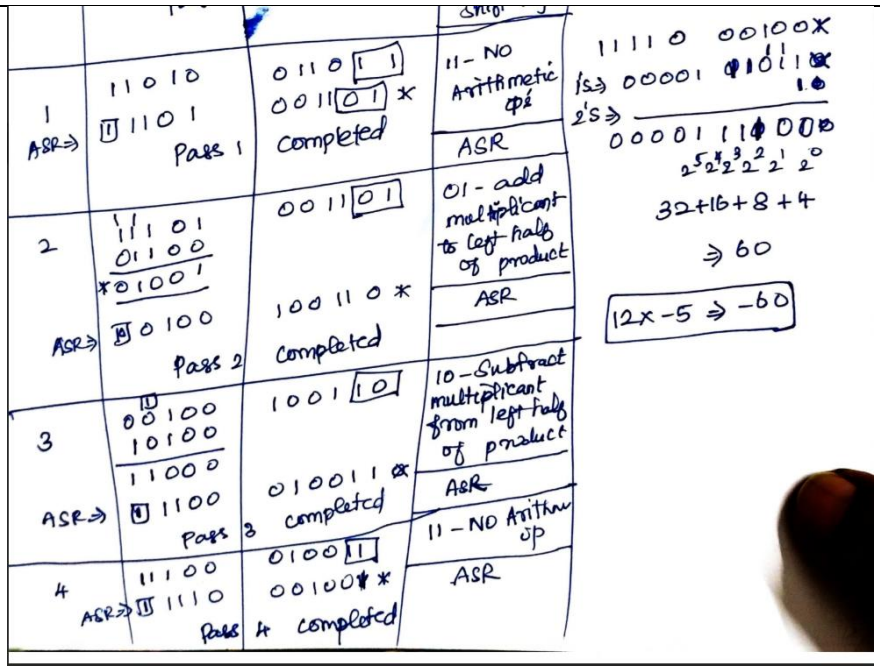
We need enough bits to represent ±12 and ±5.

Using **5-bit 2's complement**:

- **+12** = `01100`
- **−5** = 2's complement of `00101`
  → invert: `11010`
  → add 1: `11011`



SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026



b) Describe the structure and components of IEEE 754 single-precision and double-precision floating-point formats with neat diagrams.

2

3

- **IEEE 754 single precision**

$$(-1)^S \times 1.M \times 2^{(E-127)}$$

IEEE 754 Double precision

```
| Sign (1) |    Exponent (11 bits)    |     Mantissa (52 bits)     |
 bit 63        bits 62 – 52              bits 51 – 0
```

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026

	$(-1)^S \times 1.M \times 2^{(E-1023)}$				
4.	a) Consider the following instructions, classify each into the appropriate instruction set category and justify your answer: i) MOV R1, R2 ii) ADD R3, R4 iii) JMP 200 iv) IN PORT1 v) NOP vi) AND R5, R6 vii) BCD to Binary Conversion viii) LOAD R1, M[150]	3	7	1	BL 4
	b) With neat diagram, explain how CPU, Memory, and I/O devices are interconnected in a computer system.	3	3		

a) Classification of Instructions

Instruction	Category	Justification
i) MOV R1, R2	Data Transfer Instruction	Moves data from register R2 to register R1, transferring data between CPU registers.
ii) ADD R3, R4	Arithmetic Instruction	Performs addition of contents of R3 and R4, a basic arithmetic operation.
iii) JMP 200	Transfer of Control	Changes program flow by jumping to the instruction at address 200.
iv) IN PORT1	I/O Instruction	Reads data from input device or port PORT1 into CPU/register.
v) NOP	System Control Instruction	No operation; used to control timing or synchronization without changing system state.
vi) AND R5, R6	Logical Instruction	Performs bitwise AND between registers R5 and R6, used for logical operations.
vii) BCD to Binary Conversion	Conversion Instruction	Converts data from BCD format to binary, changing data representation format.
LOAD R1, M[150]	Data Transfer Instruction	Loads data from memory location 150 into register R1, transferring data into the CPU.

The **system bus** consists of three types of buses:

1. Data Bus

- Transfers **actual data** between CPU, memory, and I/O devices
- **Bidirectional**
- Width determines the amount of data transferred at a time (e.g., 32-bit, 64-bit)

2. Address Bus

- Carries the **address** of the memory location or I/O device
- **Unidirectional** (from CPU to others)
- Determines the **maximum addressable memory**

3. Control Bus

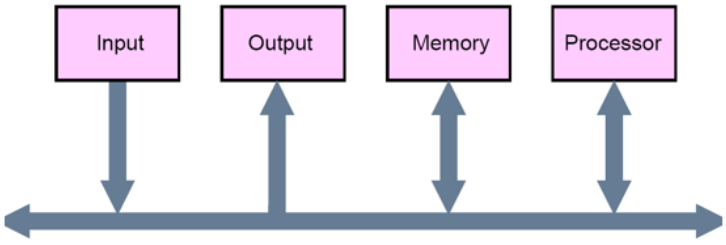
- Carries **control and timing signals**
- Coordinates operations among components
- Examples: Read, Write, Interrupt, Clock signals

Working of the Interconnection

1. The **CPU** places an address on the **address bus**.
2. Control signals (Read/Write) are sent via the **control bus**.
3. Data is transferred through the **data bus**.
4. Memory or I/O device responds based on the address and control signals.
5. I/O devices communicate with the CPU either by **programmed I/O**, **interrupts**, or **DMA**.

This answer also considered:

- A group of lines that serves a connecting path for several devices is called a bus
  - In addition to the lines that carry the data, the bus must have lines for address and control purposes
  - The simplest way to interconnect functional units is to use a single bus, as shown below



- The devices connected to a bus vary widely in their speed of operation
  - Some devices are relatively slow, such as printer and keyboard
  - Some devices are considerably fast, such as optical disks

	• Memory and processor units operate are the fastest parts of a computer
	• Efficient transfer mechanism thus is needed to cope with this problem
	  • A common approach is to include buffer registers with the devices to hold the information during transfers
	  • Another approach is to use two-bus structure and an additional transfer mechanism
	  • A high-performance bus, a low-performance, and a bridge for transferring the data between the two buses. ARMA Bus belongs to this structure				

5.	Convert the following expression into assembly instructions for 0,1,2,3 address formats and calculate the total memory traffic:
	
	P=(Q×R)−S
	
	Use the same assumptions:
	
	• Address: 2 bytes
	• Data: 2 bytes
	• Opcode: 8 bits
	• Word length: 1 byte
	
	Step 1: 0-Address Machine (Stack Machine)
	
	0-address machines are **stack-based**. Operands are pushed onto the stack, operations pop operands and push the result.
	
	Assembly Code (0-address):
	
	css Copy code
	`PUSH Q ; Push Q onto stack`
	`PUSH R ; Push R onto stack`
	`MUL ; Pop Q,R -> multiply -> push result`
	`PUSH S ; Push S onto stack`
	`SUB ; Pop (Q*R), S -> subtract -> push result`
	`POP P ; Store result into P`
		3	10	1	BL 4

Step 2: 1-Address Machine (Accumulator Machine)

1-address machine uses an **accumulator (AC)**. Operations mostly involve **AC and memory**.

Assembly Code (1-address):

```
powershell

LOAD Q        ; AC <- Q
MUL R         ; AC <- AC * R
SUB S         ; AC <- AC - S
STORE P       ; P <- AC
```

Step 3: 2-Address Machine

2-address machine: Typically **ADD R1,R2** → R1 = R1 + R2

Assembly Code (2-address):

```
powershell

MOV AC, Q     ; AC <- Q
MUL AC, R     ; AC <- AC * R
SUB AC, S     ; AC <- AC - S
MOV P, AC     ; P <- AC
```

Memory Traffic Calculation:

Step 4: 3-Address Machine

3-address machine: Each instruction can have **two source operands and one destination operand**.

Assembly Code (3-address):

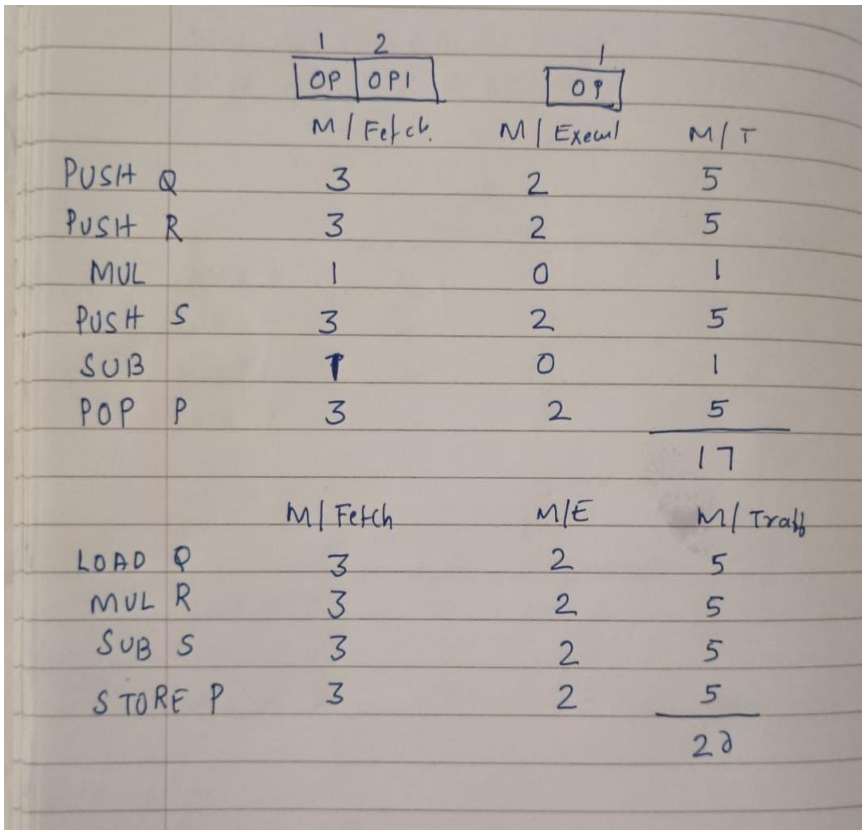
```
pgsql

MUL Q, R, TEMP   ; TEMP = Q * R
SUB TEMP, S, P    ; P = TEMP - S
```

Memory Traffic Calculation:

Instruction	Memory Access
MUL Q,R,TEMP	2 reads (Q,R) + 1 write (TEMP) = 3×2 bytes = 6 bytes?
SUB TEMP,S,P	2 reads (TEMP,S) + 1 write (P) = 3×2 bytes = 6 bytes?

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026



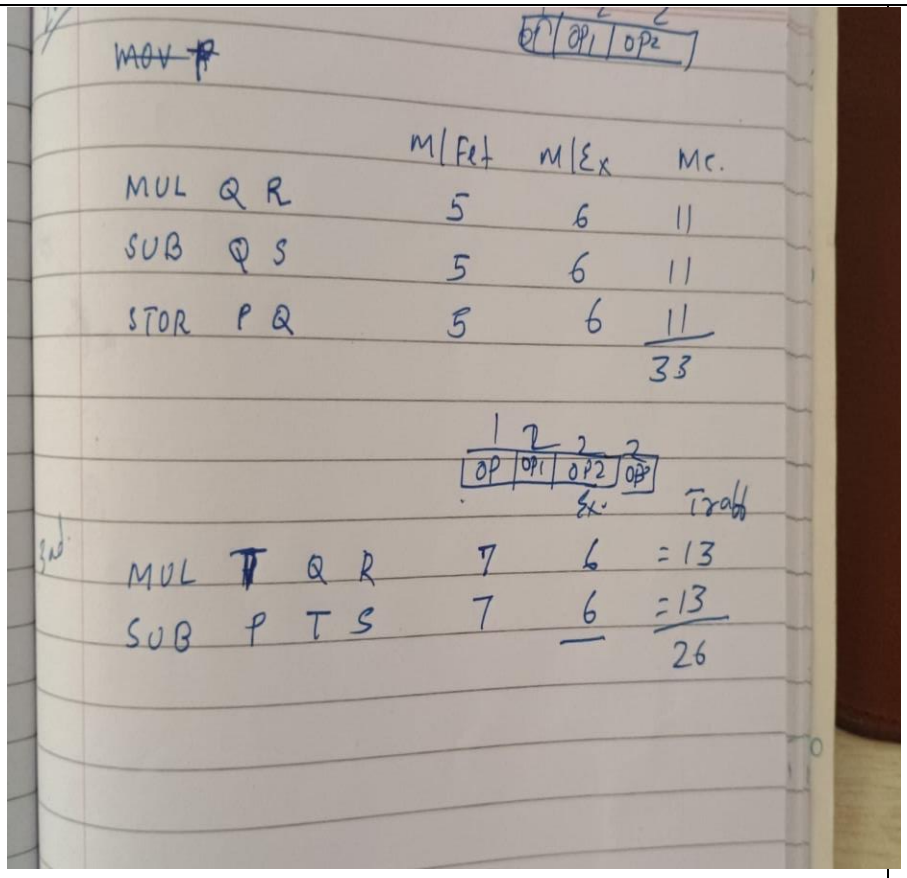
	M/Fetch.	M/Execn	M/T
PUSH Q	3	2	5
PUSH R	3	2	5
MUL	1	0	1
PUSH S	3	2	5
SUB	1	0	1
POP P	3	2	5
			17

	M/Fetch	M/E	M/Trafn
LOAD Q	3	2	5
MUL R	3	2	5
SUB S	3	2	5
STORE P	3	2	5
			20

REG.NO.:

SLOT: A2+TA2

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026



****