Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)
CHENNAI

Reg. Number:	

Continuous Assessment Test (CAT) – II October 2025

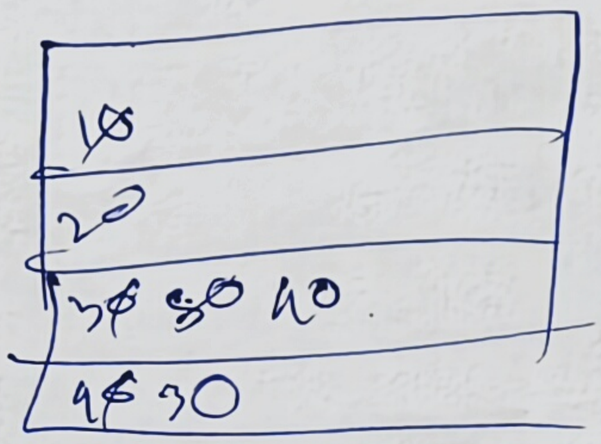
Programme	:	B. Tech (CSE and all Specializations)	Semester	:	FALL 25-26
Course Code & Course Title	:	BCSE205L-Computer Architecture and Organization	Slot	:	D1 +TD1
Faculty	:	Dr. MANJULA V Dr. KAJA MOHIDEEN A Dr. ASWIGA Dr. REVATHI A R Dr. PADMA J	Class Number	:	CH2025260100953 CH2025260100954 CH2025260100955 CH2025260100956 CH2025260100957
Duration	:	90 Minutes	Max. Mark		50 Marks

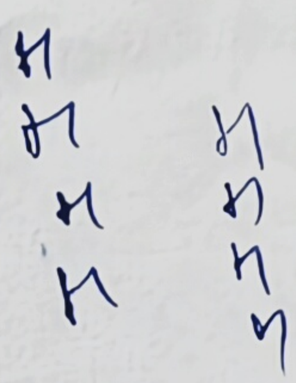
General Instructions

- Write only your registration number on the question paper in the box provided, and do not write other information
- Use statistical tables supplied from the exam cell as necessary
- Use graph sheets supplied from the exam cell as necessary
- Only a non-programmable calculator without storage is permitted

Answer all questions

Q. No	Sub Sec.	Description	Marks	CO	BT Level
1	a	Consider three different processors, P1, P2, and P3, that execute the same instruction set. Processor / Clock rate / CPI P1 / 3 GHz / 1.5 P2 / 2.5 GHz / 1.0 P3 / 4 GHz / 2.2 i. Which processor has the highest performance? (4 Marks) ii. If each processor executes a program in 10 seconds, find the number of cycles and the number of instructions. (3 Marks) iii. When you try to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. Determine the clock rate required to achieve this time reduction. (3 Marks)	10	2	K3
1	b	i. Compare the Hardwired and Microprogrammed control units in terms of their suitability for implementing 30 additional instructions in a CPU. Which control path approach is easier to add new instructions to? Justify your answer. (2 Marks) ii. Discuss the key differences between the two approaches. (3 Marks)	05	2	K3
2		A fully associative cache has 4 blocks (block size = 1 word). The cache is initially empty. The memory reference string (decimal addresses) is 10, 20, 30, 40, 10, 20, 10, 50, 20, 30, 10, 20, 30, 40, 10 i. Simulate the cache contents for FIFO replacement policy. (2 Marks) ii. Simulate the cache contents for LRU replacement policy. (2 Marks) iii. Compute the hit ratio and miss ratio for both FIFO and LRU. (2 Marks)	10	2	K3





		iv. Compute compulsory miss and conflict miss for both FIFO and LRU. (2 Marks) v. Which policy gives a better hit ratio for this reference string? Explain why the results differ. (2 Marks)			
3		A microcomputer system requires a total of 512K × 32 byte-addressable RAM. RAM chips available are 64K × 8 each. Design an interleaved memory system based on the following requirements: i. The total number of RAM chips required; the number of RAM banks required to support memory interleaving. Also, calculate the number of RAM chips per bank. (3 Marks) ii. How many address lines are needed to select the bank, and decoder logic with appropriate illustrations (3 Marks) iii. If the system is expanded to 1 M × 32 RAM using the same chips, how will the number of banks and chips per bank change? (4 Marks)	10	2	K3
4	a	A critical goal in modern embedded systems design is maximizing CPU throughput and minimizing power consumption during high-volume data transfers. Analyse the architectural role of a Direct Memory Access Controller within a Microcontroller Unit by addressing the following i. Describe the three key registers the CPU must program into the DMA Controller to initiate a transfer between a peripheral and RAM. (5 Marks) ii. Recommend which mode of transfer is preferred for time-critical, high-bandwidth communication. Justify your choice. (5 Marks)	10	2	K3
	b	Analyze the two fundamental I/O communication models used below for interfacing a microcontroller with a sensor and a display. The sensor and display are mapped to the microcontroller's memory address space for access. The sensor and output device are accessed via dedicated ports from the microcontroller's memory space i. Identify the communication mechanism for each method described above. (2 Marks) ii. Write instructions for the following operations within each model and recommend the best approach for modern embedded systems with a technical justification. • Reading data from the sensor. • Writing data to the display. (3 Marks)	05	2	K3
		********** All the best **********			