REG.NO.: 23BIT0

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

School of Computer Science Engineering and Information Systems
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2024-2025

SLOT: A1+TA1

Programme Name & Branch	**: BTECH IT**
Course Code and Course Name	**: Computer Architecture and Organization & BITE301L**
Faculty Name(s)	**: Dr. M. Angulakshmi, Dr. M. Vanitha ,Dr. M. Deepa**
Class Number(s)	**: VL2024250502702, VL2024250502721, VL2024250502716**
Date of Examination	**: 16-Mar-2025**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (2– Understand, 3 – Apply)
- CO3- Analyse the arithmetic algorithms to perform ALU operations
- CO4- Design a memory system on understanding the chip organization and analyse its performance

Q. No	Question	M	CO	BL
1	Demonstrate the step-by-step multiplication process using Booth multiplication algorithm when the following numbers are multiplied. A = + 36 (Multiplicand) B = -34 (Multiplier). Use 7-bit registers for storing the values.	10	3	3
2	a. Divide the following unsinged numbers using the Restoring division algorithm. Assume Dividend as 47 and Divisor as 12.	6	3	3
	b. Find the floating number for given single precision IEEE format 0 | 10000101 | 01010100100000000000000 Sign Exponent Mantissa	4		
3	A computer employs RAM chips of 512*8 and ROM chips of 512*8. The computer system needs 1024*8 bytes of RAM, 1024 x 16 of ROM, and two interface units with 1024 registers each. a. Draw the memory address map for the system. b. How many lines must be decoded for chip select? c. Draw the memory chip connection diagram	3 4 5	4	3
4	a. A digital computer has a memory unit of 128K and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the Tag, Cache line and Block offset of the cache memory address format?	3	4	3
	b. Consider a fully associative mapped cache of size 128 KB with block size 1024 bits. There are 17 bits in the tag. Find the Size of main memory.	3		

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	c. Consider a 4-way set associative mapped cache with block size 4 KB. The size of main memory is 16 GB and there are 10 bits in the tag. Find the Size of cache memory.	4		
05	Consider the following page reference string: 9,8,5,4, 5, 6, 7, 5, 4, 8, 9, 5, 4, 6, 7, 9, 4,6, 3. How many page faults would occur for the following replacement algorithms, assuming 3 frames? Remember all frames are initially non-empty, with values of 9, 8, and 2 in frames 1, 2, and 3, respectively. a. LRU b. FIFO c. Optimal	 3 3 4	4	2

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