SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

Programme Name & Branch : **B.Tech. (CBS)**
Course Code and Course Name : **CBS1004 Computer Architecture and Organization**
Faculty Name(s) : **R M Brisilla**
Class Number(s) : **VL2025260103255**
Date of Examination :**06/10/2025**
Exam Duration : **90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes:
  1. Provide fundamentals on machine instructions and addressing modes
  3. Analyse the performance of various memory modules in memory hierarchy
  4. Compare and contrast the features of RAID architectures of organization and structure of disk drives

Q. No	Question	Module	Marks	CO	BL
1	A pipeline consists of 4 stages with execution times of 50 ns, 30 ns, 40 ns, and 60 ns. The latch delay is 10 ns. Since the pipeline cycle time is determined by the stage with the maximum delay, calculate the following: i) Pipeline cycle time ii) Non-pipelined execution time for a single instruction iii) Speed-up ratio iv) Total execution time for 100 instructions in the pipeline v) Throughput of the pipelined execution	2	**10**	1	3
2.	A 32-bit computer employs RAM chips of size 1024 × 8 and ROM chips of size 1024 × 4. The computer system needs 2K × 16 bytes of RAM, and 2K × 8 bytes of ROM, along with 4 interface units of 256 registers each. **(a)** How many RAM and ROM chips are needed? **(b)** Draw the memory address map for the system. **(c)** How many lines must be decoded for chip select? **(d)** Draw the memory chip connection diagram.	4	**10**	3	3
3.	a) Apply the block replacement algorithm (FIFO and LRU) on the sequence of block references provided, considering a fully associative cache of size 256 bytes with block size 64 bytes. The sequence is as follows: 5, 6, 6, 4, 11, 5, 0, 6, 6, 0, 11, 6, 3, 5. For the given sequence suggest the best policy. **Summarize the details**	4	**6**	3	3

Algorithm	FIFO	LRU
Number of Hits		
Number of Misses		
Total Number of references		
Hit Ratio		

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	Miss Ratio			
	b) Consider a 2-level memory hierarchy consisting of a single-level cache and main memory. Cache access time = 20 ns, main memory access time = 100 ns. Out of 10,000 memory accesses, 7,000 times the requested word is found in cache. Assume that on a miss the block is transferred from main memory to cache and then the word is accessed from cache. What is the miss penalty, hit ratio and the effective access time of the memory system?			
4.	A company is designing an autonomous delivery robot that uses a microprocessor-based control system. The robot needs to: • Continuously read data from multiple sensors (ultrasonic sensors, GPS, and cameras) to avoid obstacles and navigate. • Communicate with a remote server to receive updated delivery routes. • Stream video from its camera to a monitoring station in real time. • Control motors to drive the wheels and robotic arm. a) Compare the trade-offs between programmed I/O, interrupt-driven I/O, and DMA in the context of this robot's tasks. b) For each method, identify which task (sensing, communication, video streaming, or motor control) it is most suitable for and explain why. c) If system resources are limited, justify how the designer should prioritize the choice of I/O method to balance real-time performance and efficiency.			1
5.	In a hospital patient monitoring system, a microprocessor is connected to several devices: • Heart rate sensor (high priority – must be serviced immediately), • IV drip monitor (medium priority – checked periodically), • Alarm buzzer (highest priority – must override all others in case of emergency), • Display unit (low priority – updates every few seconds). During operation, these devices often generate interrupts simultaneously. a) Describe how the microprocessor can manage multiple interrupts generated at the same time. b) Compare the effectiveness of polling, fixed priority, daisy chain priority, and vectored interrupt methods in this scenario. c) Justify which method would ensure real-time responsiveness for the alarm and critical medical sensors.			1

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