REG.NO.:

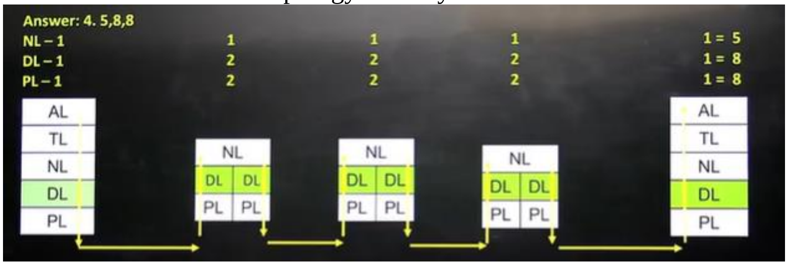
SLOT: F1+TF1

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
FALL SEMESTER 2025-2026

Programme Name & Branch : B.Tech (CSE)
Course Code and Course Name : BCSE308L Computer Networks
Faculty Name(s) : ALL
Class Number(s) : ALL
Date of Examination :
Exam Duration : 90 minutes **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes: (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)
  CO1. Interpret the different building blocks of Communication network and its architecture.
  CO2. Contrast different types of switching networks and analyze the performance of network
  CO3. Identify and analyze error and flow control mechanisms in data link layer.

Q. No	Question	M	CO	BL
1.	a) Investigate following network functionalities with respect to OSI layers i. Reliability in terms of fault tolerance, speed matching and data integrity ii. Data segmentation and reassembly iii. Data delivery with respect to node, host and process Justify the functionality mapping with the respective layers. *Fault tolerance with respect to path –network layer by packet switching and routing* *Speed matching – Link layer and transport layer takes care of flow and congestion control* *Data Integrity – Link layer and transport layer takes care of error detection using CRC and checksum* *Data segmentation and reassembly – transport layer does segmentation and reassembly and router also does fragmentation based on MTU* *Data delivery with respect to node by using MAC address at link layer* *Data delivery with respect to host by using IP address at network layer* *Data delivery with respect to process by using port number at transport layer* b) Assume that a source in India and destination in Silicon Valley are connected through three intermediate routers in between. Determine how many times each packet has to visit transport layer, network layer, data link layer and physical layer respectively during a transmission from source to destination. Illustrate the topology with layers at each node.  TL - 2	7 3	1	2

2.	a) Suppose there is exactly one packet switch between a sending host and a receiving host. The transmission rates between the sending host and the switch and between the switch and the receiving host are R1 and R2, respectively. Assuming that switch uses store and forward message switching, what is the end to end delay to send a packet of length L? (Ignore Queuing, Propagation delay and Processing delay) At time t_0 the sending host begins to transmit. At time $t_1 = L/R_1$, the sending host completes transmission and the entire packet is received at the router (no propagation delay). Because the router has the entire packet at time t_1, it can begin to transmit the packet to the receiving host at time t_1. At time $t_2 = t_1 + L/R_2$, the router completes transmission and the entire packet is received at the receiving host (again, no propagation delay). Thus, the end-to-end delay is $L/R_1 + L/R_2$. b) Suppose host A wants to send a large file to host B. The path from host A to host B has three links, of rates R1=500 kbps, R2=2Mbps, and R3=1Mbps. i. Assuming no other traffic in the network, what is the throughput for the file transfer? ii. Suppose the file is 4 million bytes. Dividing the file size by the throughput, roughly how long will it take to transfer the file to host B? iii. Analyse the throughput and delay, if R2 is reduced to 100 Kbps. *a) 500 kbps* *b) 4*10 power 6*8 = 32000000/500000 = 64 seconds* *c) 4*10 power 6 * 8 = 32000000/100000 = 320 seconds* c) How long does it take a packet of length 1000 bytes to propagate over a link of distance 2,500 km, propagation speed of $2.4 * 10^8$ m/s, and transmission rate of 2 Mbps? Does this delay depends on the packet length and transmission rate? *10 msec, d/s, no, no* d) Investigate the parameters: Transmission rates, Propagation Delay and Packet Size for the following scenarios: **Scenario 1:** Sender finishes transmitting before the first bit of the packet reaches the receiver **Scenario 2:** First bit of the packet reaches the receiver before the sender finishes transmitting *Scenario 1: 1000km, 1Mbps, 100 bytes* *Scenario 2: 100km, 1Mbps, 100 bytes*	2 3 2 3	2	3
3.	Suppose users share a 2 Mbps link. Also suppose each user transmits continuously at 1 Mbps when transmitting, but each user transmits only 20 percent of the time. i. When circuit switching is used, how many users can be supported? ii. Suppose packet switching is used, why will there be no queuing delay before the link if two or fewer users transmit at the same time. Why will there be a queuing delay if three users transmit at the same time? iii. Find the probability that a given user is transmitting. iv. Suppose now three users, find the probability that at any given time, all three users are transmitting simultaneously. Find the fraction of time during which the queue grows.	2 3 2 3	2	3

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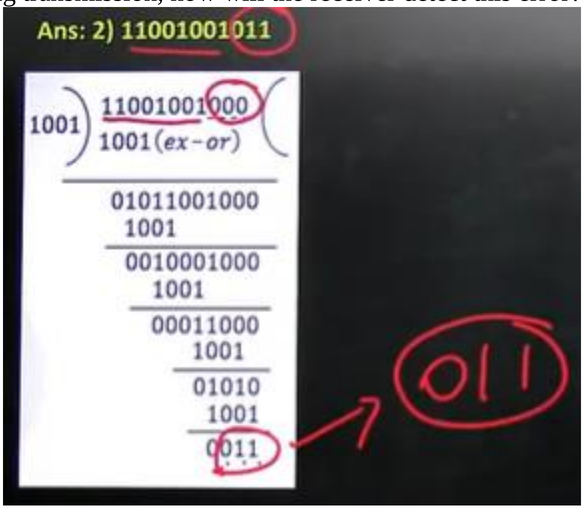
	a) 2 users can be supported because each user requires half of the link bandwidth. b) Since each user requires 1Mbps when transmitting, if two or fewer users transmit simultaneously, a maximum of 2Mbps will be required. Since the available bandwidth of the shared link is 2Mbps, there will be no queuing delay before the link. Whereas, if three users transmit simultaneously, the bandwidth required will be 3Mbps which is more than the available bandwidth of the shared link. In this case, there will be queuing delay before the link. c) Probability that a given user is transmitting = 0.2 d) Probability that all three users are transmitting simultaneously = $\binom{3}{3}p^3(1-p)^{3-3}$ $= (0.2)^3 = 0.008$. Since the queue grows when all the users are transmitting, the fraction of time during which the queue grows (which is equal to the probability that all three users are transmitting simultaneously) is 0.008.			
4.	The message **11001001** is to be transmitted using CRC polynomial x^3+1 to protect it from errors. Calculate the CRC and the message to be transmitted. Suppose the third bit from the left is inverted during transmission, how will the receiver detect this error?  *Non zero remainder on receiver side detects error.*	10	3	4
5.	a) Illustrate how hamming code can be used to detect and correct **1 bit error** at **data bit position 3** for the message **00111001**. **<u>Illustration of hamming SEC code with an example</u>** **<u>Sample 8b word and 4b check bits calculated</u>** Let us verify that this scheme works with an example. Assume that the 8-bit input word is 00111001, with data bit D1 in the rightmost position. The calculations are as follows: $C1 = 1 \oplus 0 \oplus 1 \oplus 1 \oplus 0 = 1$ $C2 = 1 \oplus 0 \oplus 1 \oplus 1 \oplus 0 = 1$ $C4 = 0 \oplus 0 \oplus 1 \oplus 0 = 1$ $C8 = 1 \oplus 1 \oplus 0 \oplus 0 = 0$	6 4	3	4

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Error in data bit 3 and re calculation of check bits

Suppose now that data bit 3 sustains an error and is changed from 0 to 1. When the check bits are recalculated, we have

$$C1 = 1 \oplus 0 \oplus 1 \oplus 1 \oplus 0 = 1$$
$$C2 = 1 \oplus 1 \oplus 1 \oplus 1 \oplus 0 = 0$$
$$C4 = 0 \oplus 1 \oplus 1 \oplus 0 = 0$$
$$C8 = 1 \oplus 1 \oplus 0 \oplus 0 = 0$$

Comparison of check bits and syndrome word generation for SEC

When the new check bits are compared with the old check bits, the syndrome word is formed:

	C8	C4	C2	C1
	0	1	1	1
⊕	0	0	0	1
	0	1	1	0

The result is 0110, indicating that bit position 6, which contains data bit 3, is in error.

Illustration by bit arrangement and check bit calculation

Figure 5.10 illustrates the preceding calculation. The data and check bits are positioned properly in the 12-bit word. Four of the data bits have a value 1 (shaded in the

Bit position	12	11	10	9	8	7	6	5	4	3	2	1
Position number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Data bit	D8	D7	D6	D5		D4	D3	D2		D1		
Check bit					C8				C4		C2	C1
Word stored as	0	0	1	1	0	1	0	0	1	1	1	1
Word fetched as	0	0	1	1	0	1	1	0	1	1	1	1
Position number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Check bit					0				0		0	1

Figure 5.10 Check Bit Calculation

table), and their bit position values are XORed to produce the Hamming
which forms the four check digits. The entire block that is stored is 0011010
pose now that data bit 3, in bit position 6, sustains an error and is changed f
The resulting block is 001101101111, with a Hamming code of 0111. An X
Hamming code and all of the bit position values for nonzero data bits resu
The nonzero result detects an error and indicates that the error is in bit pos

b) Suggest and illustrate the strategy to use hamming code to handle burst errors in a **32 bit**

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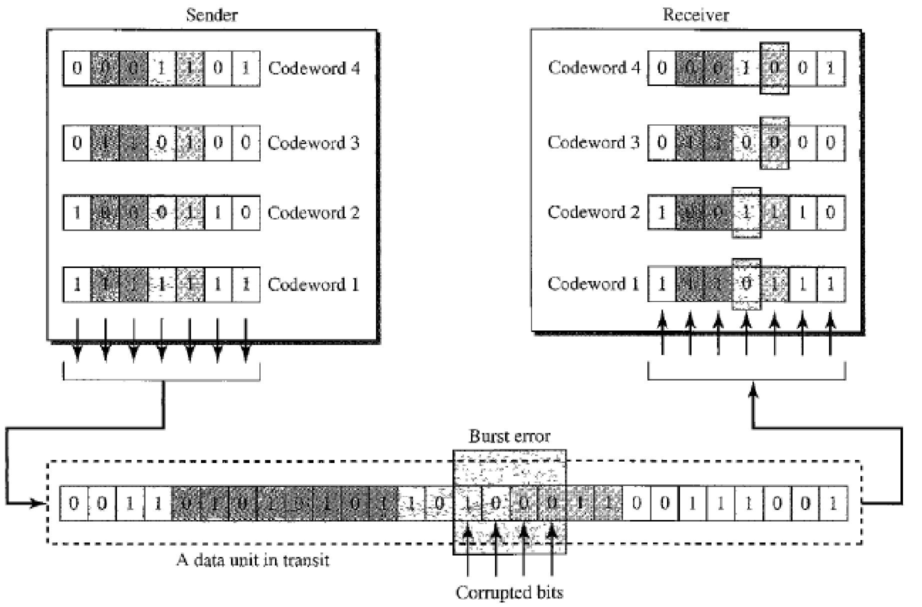
message, as single bit errors. Assume **data word size of 8 bits**.

Divide the message into data word of size 8 bits and send column by column

Figure 10.13 *Burst error correction using Hamming code*



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