VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.: 24MID0165

SLOT: A1 + TA1

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

Programme Name & Branch	: Integrated M.Tech - CSE (MIC & MID)
Course Code and Course Name	: CSI1004 & Computer Organization and Architecture
Faculty Name(s)	: Dr.Vijaya Kumar K, Mr. Kameshwaran G, Dr.M.A.Berlin
Class Number(s)	: VL2025260102476, VL2025260102481, VL2025260102482
Date of Examination	: 05-10-2025
Exam Duration	: 90 minutes Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes:
  2. Illustrate various binary data representations for fixed and floating point data. Validate efficient algorithm for arithmetic operations.
  3. Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Get the idea about different external storage devices.
  4. Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and Differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.

Q. No	Question	Module	Marks	CO	BL
1.	Illustrate the operation corresponding to Restoring division algorithm. Then, compute the division operation of 12 and 11 using Restoring method, and describe all the intermediate steps involved in the procedure.	3	10	2	BL3
2.	A computer employs RAM chips of 256 x 8 and ROM chips of 128 x 8. The computer system needs 256 *16 bytes of RAM, 256 *8 bytes of ROM, and four interface units with four registers in each. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers. a. How many RAM and ROM chips are needed? b. Draw a memory-address map for the system. c. Give the address range in hexadecimal for RAM, ROM, and interface. d. Develop a chip layout for the above said specifications.	4	10	3	BL3
3.	Assume a cache with a capacity of three frames. Analyze the given memory reference sequence using First in First out (FIFO), Least Recently Used (LRU) and Optimal Replacement strategies. Determine the final cache contents and compute the hit ratio (H) and miss ratio (M).	4	10	3	BL3

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SLOT: A1 + TA1

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

	Memory references: 1, 7, 26, 5, 2, 3, 7, 3, 2, 1, 5, 7, 12, 2, 5, 26, and 10. Assess the performance outcomes of each algorithm and justify which one offers optimal results.				
4.	a) Examine the design and operational logic underlying I/O-mapped and memory-mapped I/O approaches in modern computing systems.	5	4	4	BL2
	b) A factory uses a programmable logic controller (PLC) to manage conveyor belts, robotic arms, and emergency stop systems. Multiple sensors generate interrupts for object detection, motor overload, and emergency shutdown. During operation, an overload sensor and an emergency stop button are triggered simultaneously. The system must prioritize the emergency stop to prevent damage or injury. How should the interrupt priority be configured to ensure immediate response to the emergency stop signal? Discuss how interrupt masking could be used to temporarily suppress non-critical interrupts.		6		
5.	A high-performance computing system uses multiple processors connected to a shared system bus. Each processor may request access to the bus simultaneously to read/write data from memory or I/O devices. To avoid conflicts and ensure orderly access, a bus arbitration mechanism is implemented. Explain the role of bus arbitration techniques in this multi-processor environment.	5	10	4	BL2

****