VIT®
Vellore Institute of Technology
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REG.NO.:

SLOT:

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST – I (KEY)
FALL SEMESTER 2025-2026

Programme Name & Branch : M.Tech Integrated(CSE)
Course Code and Course Name : CSI1004 & Computer Organization and Architecture
Date of Examination : 17-08-2025
Exam Duration : 90 minutes **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes:
    1. Understand the general architecture of a computer system and the instruction based architecture.
    2. Illustrate various binary data representations for fixed and floating point data. Validate efficient algorithm for arithmetic operations.

Q. No	Question	M	CO	BL
1.	Draw IAS architecture and write an assembly language programming for the following expression using the IAS computer Instruction set and write the equivalent Register Transfer Notation. X = (A – C) / (B+D). Assume the memory locations 100, 101, 102 and 103 for A,B, C, and D respectively. Store the result in the address 105. **Key:** **Scheme of Evaluation** **S.No** | **Sub Topic** | **Marks** 1 | IAS Architecture | 3 2 | Assembly code | 3 3 | Register Transfer operation | 4 **Solution:** IAS Architecture:	10	1	2

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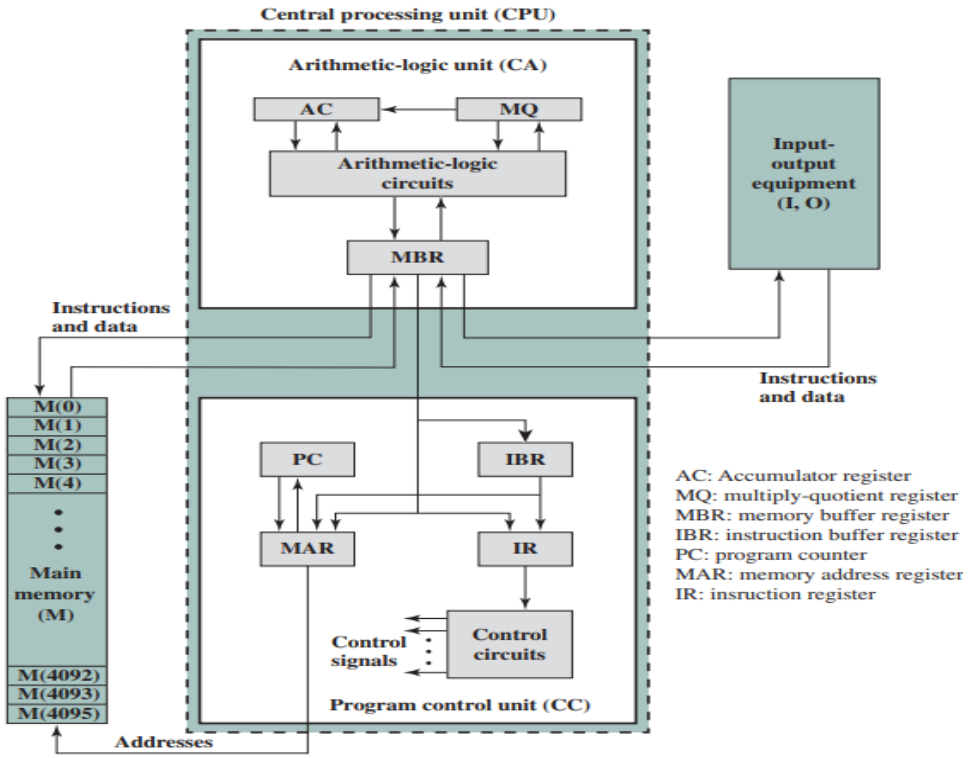

Assembly code:

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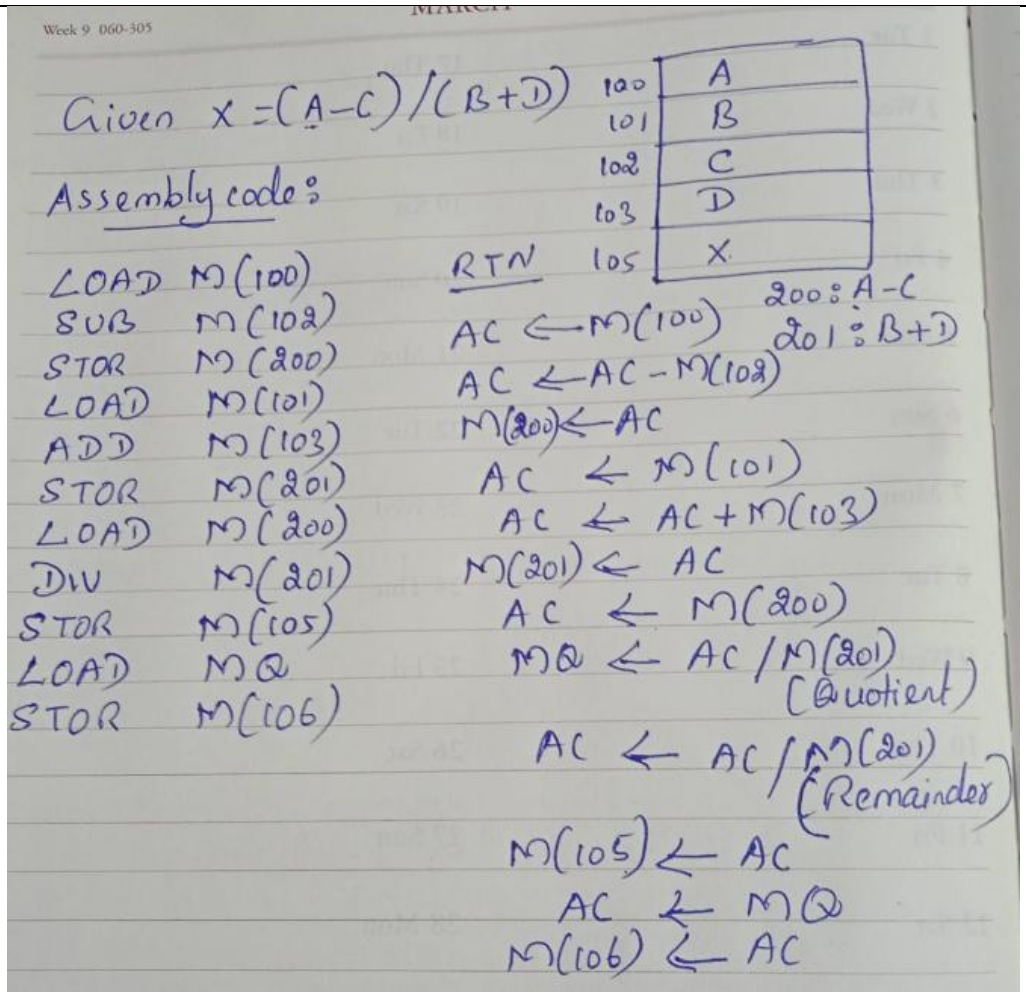

2.	Elucidate any five types of addressing modes, each with an appropriate illustrative example. A Load instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200 and Index register contains 560. Evaluate the effective address if the addressing mode of the instruction is (a) Immediate (b) Auto increment (c) Relative (d) Register indirect; (e) Auto decrement. **Key:** **Scheme of Evaluation** **S.No** / **Sub Topic** / **Marks** 1 / Explanation / 5 2 / EA Calculation / 1*5 = 5 **Solution:** **Addressing modes must be explained with an example**	10	1	2

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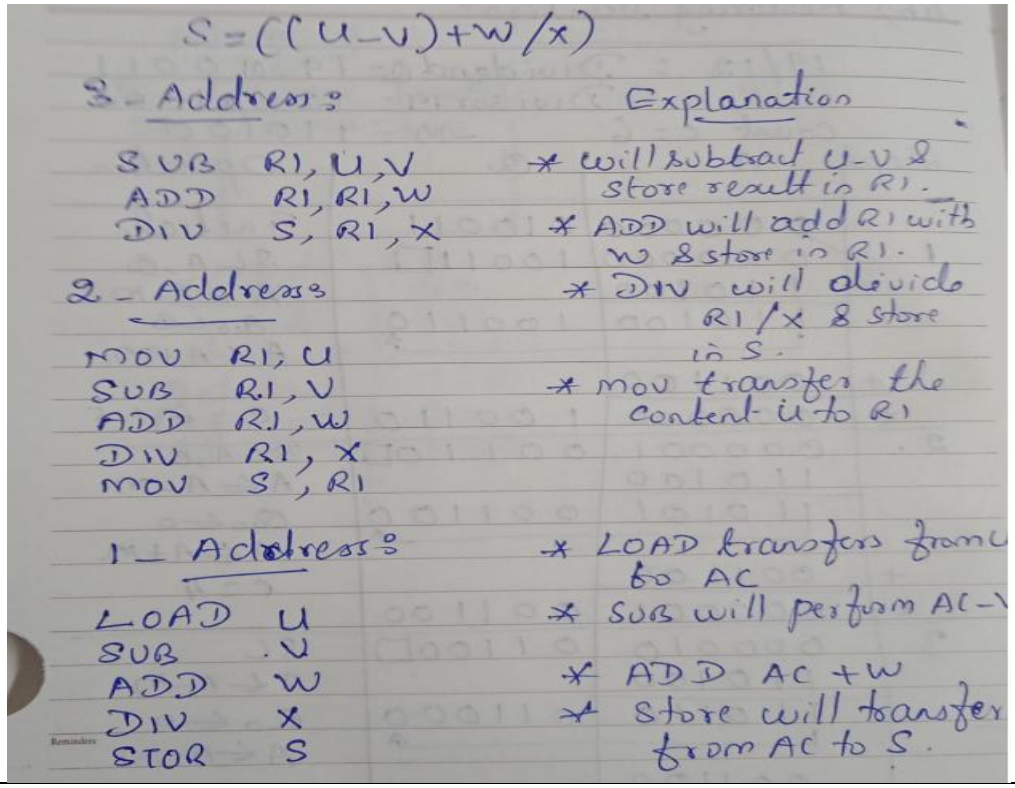
	Addressing Mode | **EA** Immediate | 301 Auto Increment | 200 Relative | 702 Register Indirect | 200 Auto Decrement | 199			

3.	Develop the assembly language program to evaluate the expression S = ((U-V)+W)/X using zero-, one-, two-, and three-address instruction formats. Provide a detailed explanation of each instruction's operational significance within its respective format.
	Key:
	Scheme of Evaluation
	S.No | **Sub Topic** | **Marks**
	1 | Instruction Formats | 7
	2 | Explanation | 3
	Solution:
	 
	S=((U-V)+W/X)
	3 - Address:
	SUB R1, U, V
	ADD R1, R1, W
	DIV S, R1, X
	2 - Address:
	MOV R1, U
	SUB R1, V
	ADD R1, W
	DIV R1, X
	MOV S, R1
	1 - Address:
	LOAD U
	SUB V
	ADD W
	DIV X
	STOR S
	Explanation
	* Will subtract U-V & store result in R1.
	* ADD will add R1 with W & store in R1.
	* DIV will devide R1/X & store in S.
	* MOV transfer the content U to R1
	* LOAD transfers from U to AC
	* SUB will perform AC-V
	* ADD AC+W
	* Store will transfer from AC to S.
		10	1	3

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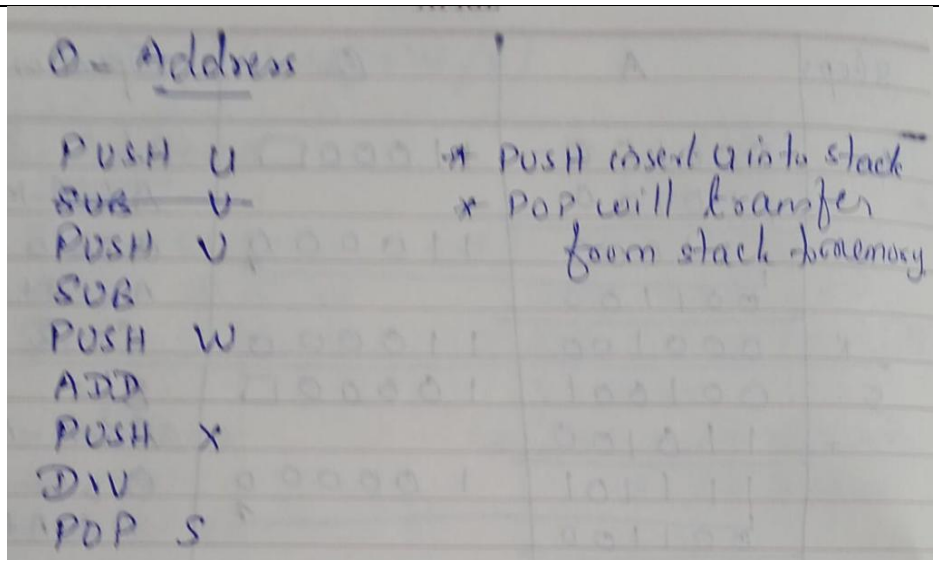
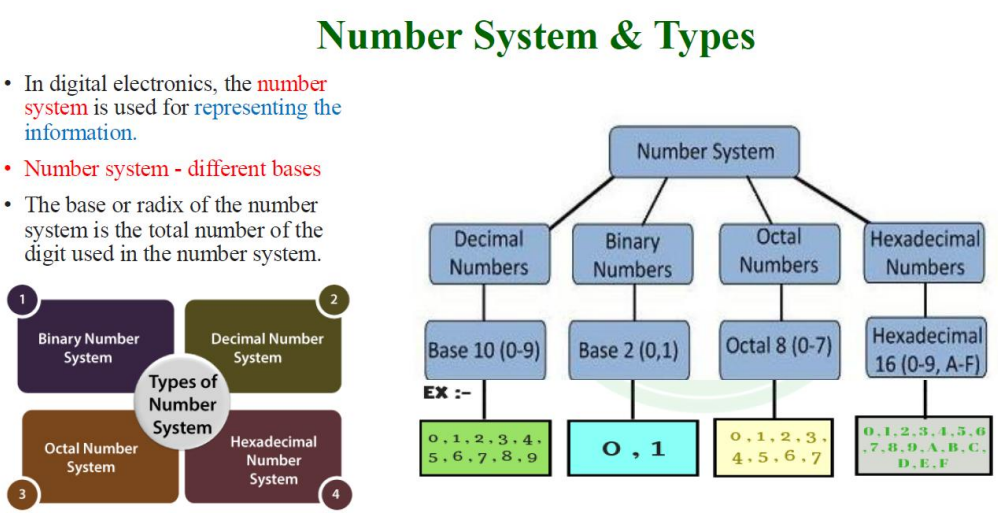
				
4.	a) Provide a detailed discussion on fixed-point number systems. Additionally, convert the Octal number $(256)_8$ and the Hexadecimal number $(AB8D)_{16}$ into binary representations. **Key:** **Scheme of Evaluation** **Solution:**  Conversion: $(256)_{10}$ ------- $(010\ 101\ 110)_2$ $(AB8D)_{16}$ ------- $(1010\ 1011\ 1000\ 1101)_2$	4	2	2
	b) Express -101.75 in IEEE 754 32-bit floating point number.	6	2	3

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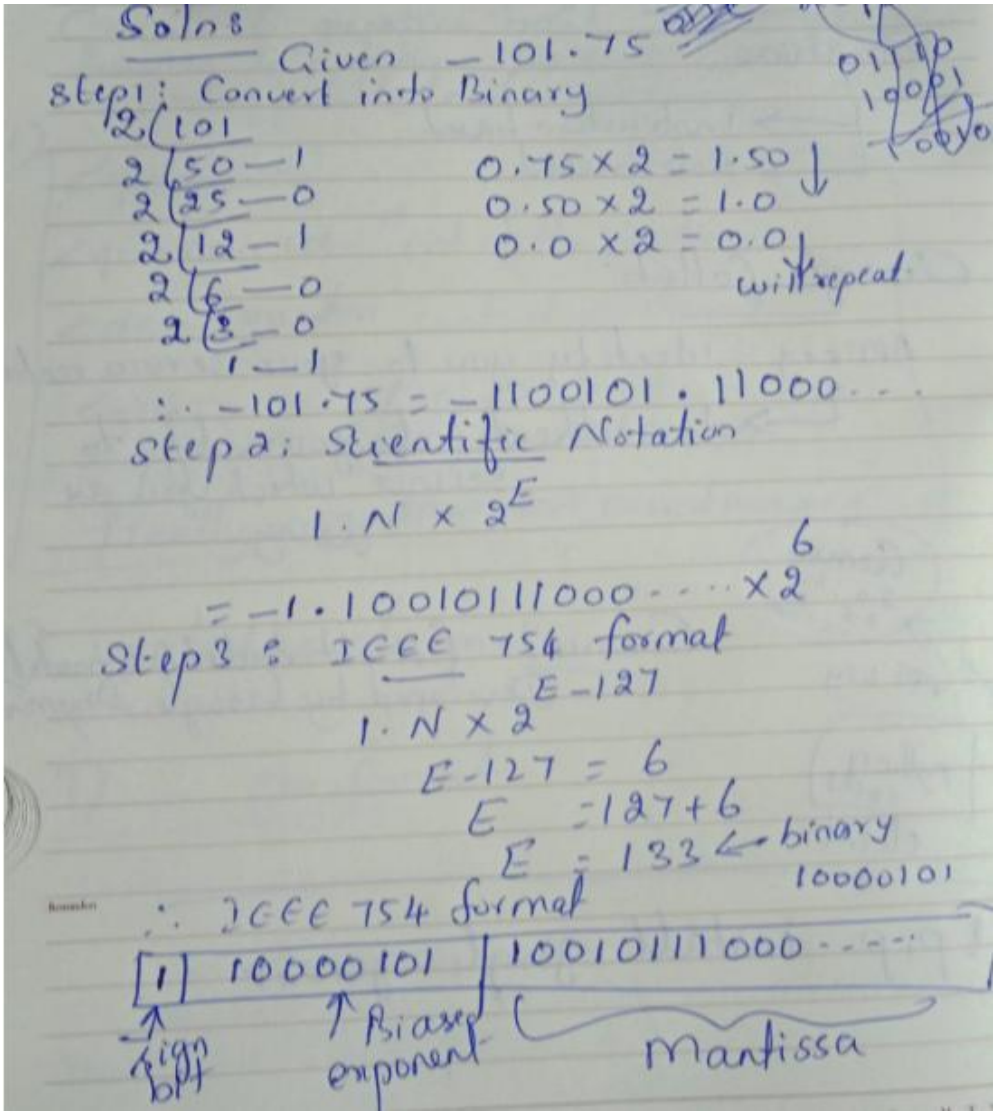
Key:
Scheme of Evaluation

S.No	Sub Topic	Marks
1	IEEE 754 Format	6

Solution:



5.	Illustrate the flowchart corresponding to Booth's multiplication algorithm. Then, compute the product of –14 and 5 using Booth's method, and present all the intermediate steps involved in the procedure. **Key:** **Scheme of Evaluation** **Solution:**	10	2	3

S.No	Sub Topic	Marks
1	Flowchart	2
2	Steps and answer	8

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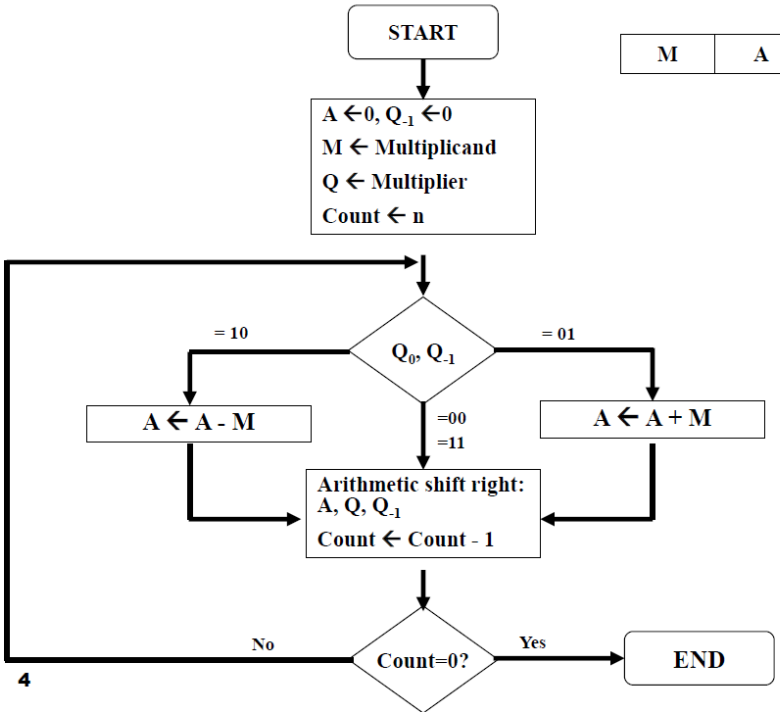
Booth's Algorithm - Flowchart



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CONTINUOUS ASSESSMENT TEST – I (KEY)
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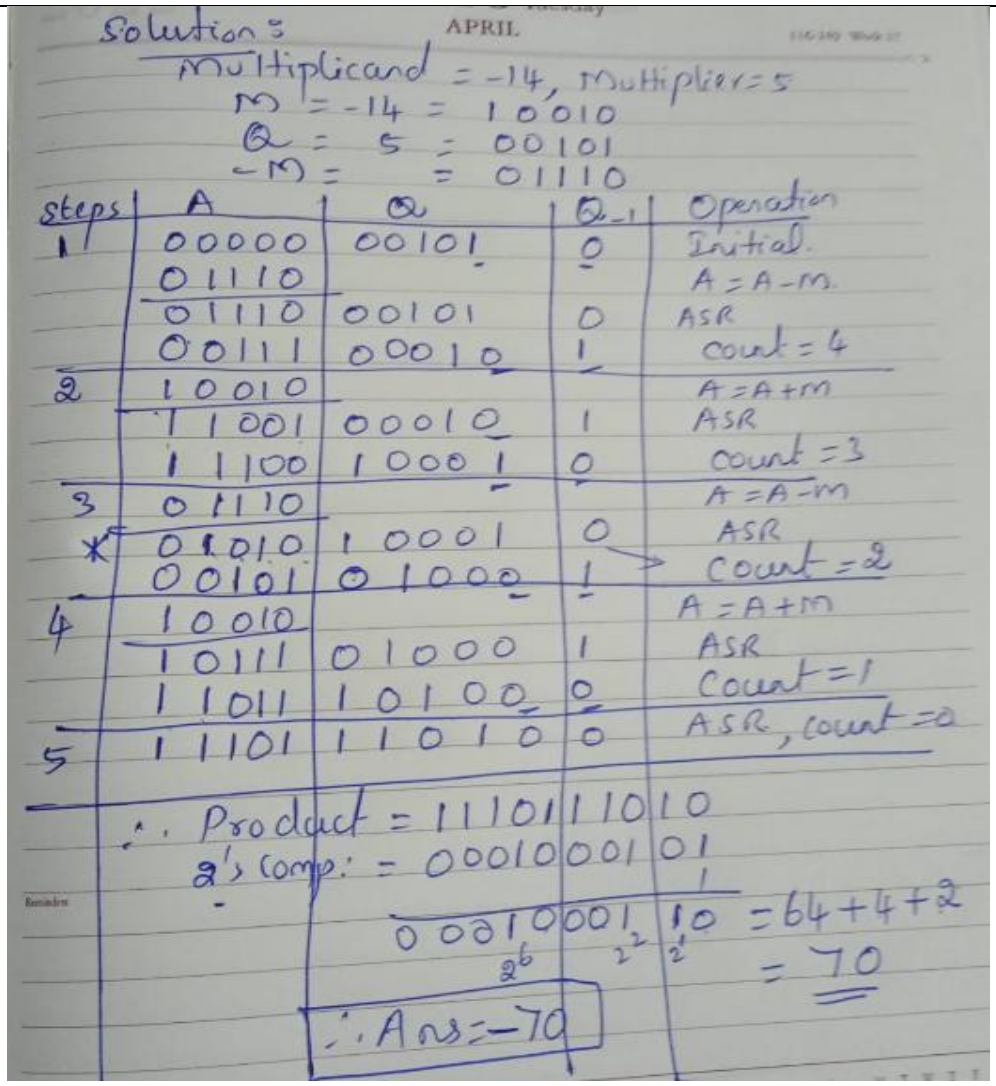

Solution:

APRIL

Multiplicand = -14, Multiplier = 5

M = -14 = 10010

Q = 5 = 00101

-M = = 01110

Steps	A	Q	Q_{-1}	Operation
1	00000	00101	0	Initial.
	01110			A = A - m.
	01110	00101	0	ASR
	00111	00010	1	count = 4
2	10010			A = A + m
	11001	00010	1	ASR
	11100	10001	0	count = 3
3	01110			A = A - m
	01010	10001	0	ASR
	00101	01000	1	count = 2
4	10010			A = A + m
	10111	01000	1	ASR
	11011	10100	0	count = 1
5	11101	11010	0	ASR, count = 0

∴ Product = 11101 11010

2's comp. = 00010 00101 + 1

00010 00110 = 64 + 4 + 2 = 70

(2^6, 2^2, 2^1)

∴ Ans = -70

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