Q/K/TY

Reg. No: 24MID0285

VIT
Vellore Institute of Technology

Final Assessment Test – November 2025

Course: CSI1004 - Computer Organization and Architecture
Class NBR(s): 2476/2481/2482
Slot: A1+TA1
Time: Three Hours
Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

COs	CO Statements
CO1	Understand the general architecture of a computer system and the instruction based architecture
CO2	Illustrate various binary data representations for fixed and floating point data. Validate efficient algorithm for arithmetic operations.
CO3	Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Get the idea about different external storage devices.
CO4	Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and Differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.
CO5	Understand some system performance enhancement techniques such as pipeline concepts, parallel execution, etc. Introduction to some of the advanced architectures.

BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Answer ALL Questions
(10 X 10 = 100 Marks)

1. With a suitable block diagram, describe the organization of a computer system based on the stored program concept. Explain its functional units in detail. **CO1 BL2**

2. Analyze how different types of registers (general-purpose, special-purpose, and control registers) coordinate with system buses (data, address, and control) to enable instruction execution. Discuss how register file size and bus width/clock synchronization impact instruction throughput, memory latency, and overall CPU performance. Provide examples from modern architectures. **CO1 BL3**

3. In what ways do fixed-length and variable-length instruction formats influence processor architecture and the complexity of instruction decoding? Use R-type, I-type, and J-type instructions from a standard RISC architecture to illustrate your explanation. **CO1 BL2**

CO1 BL4

4. Given the arithmetic expression:

$X = (A + B) * (C - D)$

Assume a one-address accumulator-based machine architecture. Memory locations A, B, C, and, D hold integer values. Additionally, pointer variables PTR1 and PTR2 reference the addresses of A, B, C, and D. Write optimized assembly instruction sequences to evaluate the expression using the following addressing modes:

i. Immediate Addressing
ii. Direct Addressing
iii. Indirect Addressing

Note: a) Clearly indicate how each addressing mode accesses operands.
b) Minimize instruction count and memory usage where possible.

5. a) A system uses a cache of size 8 KB with a block size of 64 bytes. The main memory is 64 KB. [5] CO3 BL3

Assume: Direct-mapped cache, Byte-addressable memory

i. Calculate the number of cache blocks.
ii. Determine the number of bits required for:
- Block offset
- Index
- Tag

iii. For a memory address 0x1C34, identify:
- Cache block number
- Tag value
- Block offset

b) A system has 3 page frames and uses the Least Recently Used (LRU) page replacement algorithm. Given the following page reference string: 2, 4, 1, 2, 5, 3, 2, 4, 1, 5. Simulate the page replacement process , Show the content of the page frames after each page reference and Calculate the total number of page faults. [5]

6. Explain the differences between Programmed I/O, Interrupt-driven I/O, and Direct Memory Access (DMA) in terms of CPU involvement, data transfer efficiency, and system performance. Illustrate each technique with a flowchart showing how control and data signals are managed. CO4 BL2

7. A system uses a RAID 5 configuration with 4 disks, each of 1 TB capacity. CO4 BL3

i. Calculate the total usable storage capacity.
ii. Explain how parity is distributed across the disks.
iii. Discuss how RAID 5 improves fault tolerance and read/write performance compared to RAID 0 and RAID 1.

8. Explain how pipelining enhances instruction throughput in a RISC processor. Include a diagram of a 5-stage pipeline and describe how data hazards and control hazards are handled. **CO5 BL2**

9.a) Given two 8-bit signed fixed-point numbers in 2's complement format: 01011010 and 11100100, perform both addition and subtraction. **CO2 BL4**

i. Show binary steps for both operations.
ii. Indicate if overflow occurs in either case.
iii. Convert the results to decimal.

OR

9.b) IEEE 754 Floating-Point Conversion (Single and Double Precision) **CO2 BL4**

i. Convert the decimal number **-13.625** into IEEE 754 format in both:
   1. Single-precision (32-bit)
   2. Double-precision (64-bit)

   For each format:
ii. Determine the sign bit, biased exponent, and normalized mantissa.
iii. Show all conversion steps clearly.
iv. Write the final binary representation.

10.a) Multiply -6 and 3 using Booth's algorithm with 4-bit representation. **CO2 BL4**

i. Draw the flow chart, show initialization, decision logic, shifting, and arithmetic steps.
ii. Present the final product in both binary and decimal.

OR

10.b) Divide 25 by 4 using fixed-point representation with 6-bit format. **CO2 BL4**

i. Draw the Flow chart and represent both numbers in fixed-point binary.
ii. Perform binary division using non- restoring method.
iii. Convert the result back to decimal and comment on precision loss.

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