VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SLOT: A2+TA2

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

Programme Name & Branch	**: M.Tech. (CSE, MID)**
Course Code and Course Name	**: CSI1004 Computer Organization and Architecture**
Faculty Name(s)	**: R M Brisilla, Manikandan K, Krishnamoorthy A, Siva Kumar N**
Class Number(s)	**: VL2025260102475, VL2025260102477, VL2025260102478, VL2025260102484**
Date of Examination	**: October 5, 2025**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes:
  CO 2: Illustrate various binary data representations for fixed and floating point data. Validate efficient algorithm for arithmetic operations.
  CO 3: Explain the importance of hierarchical memory organization. Able to construct larger memories. AnalyseS and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Get the idea about different external storage devices.
  CO 4: Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and Differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.

Q.No	Question	M	CO	BL
1.	Draw the flowchart for non-restoring binary division method and perform step by step operations of non-restoring binary division for 18/6.	10	2	4
2.	A computer employs RAM chips of 128 x 8 and ROM chips of 512 x 8. The computer system needs 256 x 16 of RAM, 1024 x 16 of ROM, and two interface units with 256 registers each. a. Compute total number of decoders are needed for the above system? b. Design a memory-address map for the above system c. Show the chip layout for the above design	10	3	6
3.	Consider a cache with 32 blocks and 32 bytes per block. Main memory is byte addressable with 32-bit address. With a neat sketch explain about the address formats for the following mapping techniques: a. Associative mapping b. Set Associative mapping (Assume 8-way set associative) c. Direct mapping	10	3	3
4.	A computer system uses a shared system bus for processor, memory, and multiple I/O devices. (i) Analyze how bus arbitration ensures fairness and efficiency when multiple I/O modules request the bus simultaneously. (ii) Compare the performance impact of synchronous vs. asynchronous bus communication with respect to high-speed I/O transfers.	10	4	3
5.	Evaluate the trade-offs between strobe and handshaking control signals in terms of synchronization, error handling, and hardware complexity. Suggest a hybrid scheme that combines the merits of both and illustrate the real-time I/O operation.	10	4	5