



SCHOOL OF COMPUTER SCIENCE ENGINEERING AND INFORMATION SYSTEMS
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

SLOT: C1+TC1+TCC1

Programme Name & Branch : BCA(CS)
Course Code and Course Name : UBCA102L & Computer Organization and Architecture
Faculty Name(s) : Dr. ALAGIRI I & Dr. Rajesh p
Class Number(s) : VL2025260105754 & VL2025260105745
Date of Examination : 07/10/2025
Exam Duration : 90 minutes **Maximum Marks: 50**

General instruction(s):

Answer All Questions

CO2: Apply the instruction set for problems with the design of central processing unit.

CO3: choose the various operations for computer arithmetic metrics.

Q. No	Question	M	CO	BL
1	A computer system uses a memory unit with 256 words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction format has four fields: 1. An indirect bit 2. An operation code (opcode) 3. A register code field to specify one of 64 registers 4. An address part to specify a memory word Answer the following: a) How many bits are there in the operation code, the register code, and the address part? b) Draw the instruction word format and indicate the number of bits in each field. c) How many bits are there in the data input/output lines and the address input lines of the memory? d) Give a sample binary instruction word (32 bits) and interpret its fields (indirect bit, opcode, register, address).	10	2	3
2	Convert the given infix expression into its equivalent postfix expression. Apply the proper operator precedence and associativity rules while performing the conversion. The expression is: $X = \frac{(A^B + C) \times (D - E^F)}{H \times K^F}$	10	3	3



VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SCHOOL OF COMPUTER SCIENCE ENGINEERING AND INFORMATION SYSTEMS

CONTINUOUS ASSESSMENT TEST - II

FALL SEMESTER 2025-2026

SLOT: C1+TC1+TCC1

3	Consider the following arithmetic expression: $X = \frac{(A^B + C) \times (D - E^F)}{H \times K^F}$ a) Represent the above expression in 0-address instruction format b) Represent the same expression in 3-address instruction format.	10	3	3
4	Draw the flowchart that performs both signed and unsigned binary addition, showing decisions for sign check, two's-complement conversion when needed, binary addition, and overflow/carry detection. Using that flowchart, perform step-by-step binary calculations for 9 - 10 and 10 - 9 (use 8-bit representation) and show how the algorithm proceeds at each step. For each case, display the intermediate binary forms (including the two's-complement of the subtrahend), the binary addition steps, and the resulting bit pattern. State and explain the final result for both signed and unsigned interpretations and indicate where overflow or carry occurs (if any).	10	3	4
5	Explain multiplication algorithm used for signed binary multiplication. Illustrate the algorithm by performing step-by-step multiplication of -5 and -6. Clearly show the binary representation of the numbers, the successive steps of the algorithm, and the result obtained.	10	3	4
