REG.NO. 24BEE0103

SLOT: F1+TF1

VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRICAL ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
FALL SEMESTER 2025-2026

Programme Name & Branch	**: B.Tech &EEE, EIE**
Course Code and Course Name	**: BEEE206L/Digital Electronics**
Faculty Name(s)	**:Dr.A.Sharmila and Dr.S.Balaji**
Class Number(s)	**: VL2025260101038 /VL2025260101041**
Date of Examination	**: 22/08/2025**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- Rough work should not be done on question paper. It will be treated as malpractice.
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyze, 5 – Evaluate, 6 – Create)

Course Outcomes Statements:

CO. 1: Develop digital logic circuits and apply to solve real world applications.
CO. 2: Design and analyze digital circuits using Verilog HDL.
CO. 3: Design and implement combinational circuits, sequential circuits and programmable logic devices.

Q. No	Question	M	CO	BL
1.	Convert the following functions into canonical form (i) $AB + BC'D + A'D$ (ii) $(A + B')(C' + D')(B' + C')$	5+5	1	3
2.	Using K-map, simplify the following function and obtain (i) minimal sum of products, and (ii) minimal product of sums form. $f(w, x, y, z) = \sum m(0,2,3,6,7) + \sum d(8,10,11,15)$ Realize the minimized expression using NAND and NOR logic.	10	1	2
	Design a three way light control system for the given statements. Assume a room has three doors and a switch by each door controls a single light in the room. Let A, B, and C represents the state of the switches. Assume the light is OFF if all switches are open. Closing any switch turns the light ON. Closing another switch will have to turn the light OFF. Light is ON if any one switch is closed and OFF if two (or no) switches are closed. Light is ON if all three switches are closed. Write Verilog HDL code for the minimized circuit.	10	2	3
4.	a) Design and analyse full adder circuit using gate level modelling.	5	2	3
	b) Design and analyse 3 to 8 decoder circuit using data flow modelling	5		
5.	Design and analyze BCD to Excess-3 code converter.	10	3	2