REG.NO

VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRICAL ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
FALL SEMESTER 2025-2026

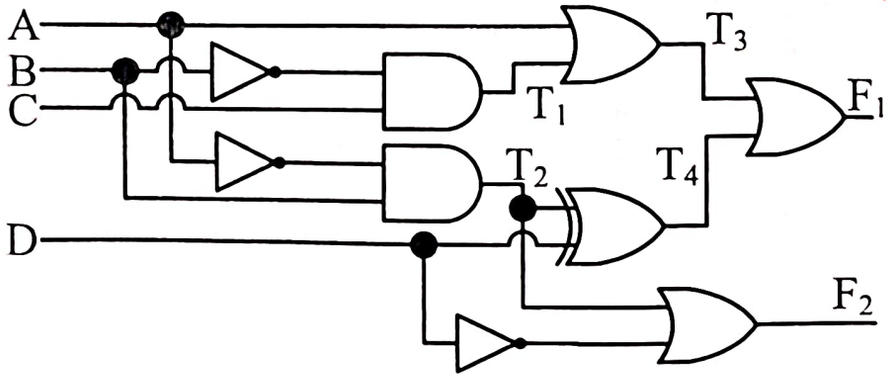
SLOT: F2+TF2

Programme Name & Branch	**: B. Tech (EEE & EI)**
Course Code and Course Name	**: BEEE206L, and Digital Electronics**
Faculty Name(s)	**: Dr. Dhanamjayulu C, Dr. Rajesh Kumar Lenka**
Class Number(s)	**: VL2025260101039, VL2025260101042**
Date of Examination	**:22/08/2025**
Exam Duration	**: 90 minutes**

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes (**Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)**
  CO1. Develop digital logic circuits and apply to solve real world applications.
  CO2. Design and analyze digital circuits using Verilog HDL.
  CO3. Design and implement combinational circuits, sequential circuits and programmable logic devices.

Q. No	Question	M	CO	BL
1.	A security system alarm starts beeping when the 4-bit binary input number represents a prime number or ends with binary 010. However, the security system is restricted to read numbers above 12. Design the digital logic circuit for the security system. Write an HDL dataflow model of the circuit.	10	1 & 2	3
2.	Design a combinational circuit that converts a four-bit BCD to Excess-3 code.	10	3	3
3.	Implement the following Boolean function with NAND and NOR gates: $F(A, B, C) = \sum(1, 2, 3, 4, 5, 7)$	10	1	3
4.	Derive the Boolean expressions for $T1$ through $T4$ as shown in Fig. 1. Evaluate the outputs $F1$ and $F2$ as a function of the four inputs. Write and verify a gate-level HDL model of the circuit.  Fig. 1	10	2	3
5.	Using the conditional operator (?:), write an HDL dataflow description of a full adder.	10	2 & 3	3

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