REG.NO.:

VIT®
Vellore Institute of Technology
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NAME OF THE SCHOOL
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

SLOT: F1+TF1

Programme Name & Branch	: B.Tech & EEE,EIE
Course Code and Course Name	: BEEE206L / Digital Electronics
Faculty Name(s)	: Dr. Balaji S & Dr. Sharmila A.
Class Number(s)	: VL2024250500928 & VL2025260101038
Date of Examination	: 10 -10-2025
Exam Duration	: 90 minutes

Maximum Marks: 50

General instruction(s): Answer All Questions

- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes:

3. Design and implement combinational circuits, sequential circuits and programmable logic devices.

Q. No	Question	M	CO	BL
1.	A BCD decoder which can light up 7 segment LED displays. It displays the BCD number and if the input is not a BCD, it displays the letter 'E'. Design and write the Verilog code for the decoder.	10	3	3
2.	A device which is a combinational circuit that uses multiple input that direct the output through single line which implements full subtractor. Design and write a Verilog code using structural level modelling to implement the same	10	3	3
3.	An L-M flip-flop works as follows: If LM = 00, the next state of the flip-flop is 1. If LM = 01, the next state of the flip-flop is the same as the present state. If LM = 10, the next state of the flip-flop is the complement of the present state. If LM = 11, the next state of the flip-flop is 0. a) Write the characteristic table and equation of LM flip-flop. b) Tabulate the excitation table of the LM flip flop. c) Construct D – flip flop from LM flip flop	10	3	4
4.	The digital system input four binary bits at once and if the input is found to be a odd number, the system is fed with input. The system output the bits one at a time over a single line otherwise. Draw the circuit diagram and describe the system with necessary timing diagram. Write an HDL behavioural modelling for the digital system.	10	3	4
5.	A sequential circuit contains three flip-flops. Initially a binary number N ($000 \leq N \leq 100$) is stored in the flip-flops. After a single clock pulse is applied to the circuit, the circuit should contain N + 011. Design the circuit using T flip-flops and verify its design by Verilog behavioural modelling	10	3	4