REG.NO.:

VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SLOT: F2+TF2

SCHOOL OF ELECTRICAL ENGINEERING
FALL SEMESTER 2025-2026
CONTINUOUS ASSESSMENT TEST - II

Programme Name & Branch	**: B. Tech & EEE/EIE**
Course Code and Course Name	**: BEEE206L and Digital Electronics**
Faculty Name(s)	**: Dr. Dhanamjayulu C/ Dr. Rajesh Kumar Lenka**
Class Number(s)	**: VL2025260101039/1042**
Date of Examination	**: 10/10/2025**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- Rough work should not be done on question paper. It will be treated as malpractice.
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Course Outcomes Statement:

CO.3: Design and implement combinational circuits, sequential circuits and programmable logic devices.

Q. No	Question	M	CO	BL
1.	The S-R flip-flop exhibits an undefined or invalid output when both S (Set) and R (Reset) inputs are high simultaneously. Analyze this condition and propose a modified design or approach to eliminate this invalid state. Justify your approach with reference to both theoretical and practical implications with a basic circuit and timing diagram.	10	03	03
2.	Draw the logic diagram to implement a T flip-flop using an SR flip-flop and explain how the inputs should be connected to achieve the toggling action. Write an HDL behavioural modelling for the digital system.	10	03	03
3.	Design a digital system using a shift register to read a serial data stream (1011) from a sensor and output the data to a digital display in parallel. Draw the circuit diagram and describe how the data is captured and presented. Write an HDL behavioural modelling for the digital system.	10	03	03
4.	A digital elevator system in a 7-floor building uses a synchronous counter to track the current floor. During testing, the system occasionally skips floors or shows unstable transitions when rapidly switching between up and down commands. Evaluate how your design ensures correct sequencing and timing in both counting modes, and propose one improvement to enhance its performance in high-speed applications. Write an HDL behavioural modelling for the digital system.	10	03	03
5.	A manufacturing line uses a counter to control a robotic arm that follows a specific sequence of operations: 000 → 101 → 011 → 001 → 110 → 100 → 010 → 111 → 000 (repeat). However, during operation, the robotic arm sometimes performs out-of-sequence actions, causing assembly errors. Evaluate how counter design choices can impact reliability, and propose a solution that ensures the robotic arm consistently follows the intended sequence, even in the presence of noise or glitches. Write an HDL behavioural modelling for the digital system.	10	03	03