A/L/TY

Reg. N

VIT
Vellore Institute of Technology

Final Assessment Test – Nov

Course: **BEEE206L** - **Digital Electronics**

Class NBR(s): **1038 / 1041**

Time: **Three Hours**

- **KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREAT**
- **DON'T WRITE ANYTHING ON THE QUESTION PAPER**

COs	CO Statements
CO1	Develop digital logic circuits and apply to solve real world applications.
CO2	Design and analyze digital circuits using Verilog HDL.
CO3	Design and implement combinational circuits, sequential circuits and programmable logic devices.
CO4	Analyze and synthesize complex digital modules and circuits for various applications.
CO5	Able to identify and prevent various hazards and timing problems in a digital design.

BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Answer ALL Questions
(10 X 10 = 100 Marks)

1. Plot the logical expression $ABCD + AB'C'D' + AB'C + AB$ on 4-variable K-map; obtain the simplified expression from the map. **CO1 BL3**

2. Minimize the given Boolean function using K-map and implement the simplified function using NAND logic. **CO1 BL3**
$F(w,x,y,z) = \sum m(0,1,2,11,15) + \sum d(8,9,14)$

3. Write the Verilog code for half subtractor using data flow, gate level and behavioural modelling. **CO2 BL3**

4. Design a 4 bit Binary to Gray code converter, and write the Verilog code for the same using data flow and gate level modelling. **CO3 BL3**

5. Implement the logic function using eight input data selector/Multiplexer. **CO3 BL3**
$F(D,C,B,A) = \sum m(1,2,5,6,7,8,10,12,13,15)$

6. Design an Octal to Binary Encoder and write the Verilog code for the same using structural modelling. **CO3 BL3**

7. Design an synchronous counter that counts through all states from 1111 down to 0000. **CO3 BL3**

8. Design a sequence detector using Mealy models that produces an output '1' whenever the non-overlapping sequence 1011 is detected. **CO4 BL3**

9.a) Write the Verilog code for SISO and SIPO shift register using behavioural modelling. **CO4 › BL3**

OR

9.b) Write the Verilog code for D Flip Flop and JK Flip Flop using behavioural modelling. **CO4 BL3**

10.a) Design an asynchronous circuit that has two inputs X_1 and X_2 and one output Z. The circuit is required to give an output whenever the input sequence (0, 0) (0,1) and (1,1) received in the same order. **CO5 BL3**

OR

10.b) Obtain the PAL and PLA structure for the following Boolean functions: **CO5 BL3**

Y3= A'BC'D+A'BCD'+A'BCD+ABCD'

Y2 = A'BCD'+A'BCD+ABCD

Y1= A'BC'+A'BC+AC+ABC'

Y0= ABCD

⇔⇔⇔ **A/L/TY** ⇔⇔⇔