Reg. Number

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)
CHENNAI

Continuous Assessment Test (CAT) – I AUGUST 2025

Programme	:	M.Tech. in Computer Science and Engineering (Data Science)	Semester	:	Winter 2025-26
Course Code & Course Title	:	IACSI202 & Digital Logic and Computer Design	Class Number	:	CH2025260501046 CH2025260501055
Faculty	:	Dr. S.A. Amutha Jeevakumari Dr.Padmavathy T V	Slot	:	B1+TB1
Duration	:	90 minutes	Max. Mark		50

General Instructions: < Use this space to provide additional information such as graph sheet, data book etc.>

- Write only your registration number on the question paper in the box provided and do not write other information
- Use statistical tables supplied from the exam cell as necessary
- Use graph sheets supplied from the exam cell as necessary
- Only non-programmable calculator without storage is permitted

Answer all questions

Q. No	Sub Sec.	Description	Marks	CO	BT Level
1		In an industrial automation system, a safety controller monitors five binary input signals: • A, B – Mode selection bits • C, D – Sensor condition indicators • E – Emergency enable signal The controller activates a critical safety output F only for specific combinations of these inputs to prevent equipment damage and ensure operator safety. Due to hardware limitations, the designer wants the logic to be implemented using the minimum number of logic gates, thereby reducing cost, power consumption, and propagation delay. During testing, it was observed that the safety output $F = 1$ for the following decimal input combinations (where inputs are ordered as A, B, C, D, E) $F(A,B,C,D,E) = \sum m(0,2,4,6,7,18,19,22,23,25,28,29)$ Minimize the given Boolean function so that it can be implemented using the fewest possible logic gates. Write the minimized Boolean expression in: (a) Simplified SOP (Sum of Products) form (5 marks) (b) Simplified POS (Product of Sums) form (5 Marks) (c) Draw the logic gate implementation diagram for the minimized SOP expression (5 Marks).	15	2	3

2		A smart digital billing machine used in a retail store internally represents each decimal digit (0–9) using a 4-bit weighted code with positional weights 8, 4, 2, and 1. However, the display module of the machine operates using a self-complementing 4-bit weighted code with weights 2, 4, 2, and 1, as it simplifies error detection and correction during transmission to the display. To ensure compatibility between the processing unit and the display unit, a combinational logic circuit is required that converts the digit from the input weighted representation (8-4-2-1) to the output weighted representation (2-4-2-1). Consider the following requirements for designing a combinational circuit: • Assume that only valid decimal digits (0 to 9) are applied at the input. • The input is provided as four binary signals: • A, B, C, D (with weights 8, 4, 2, 1 respectively). • The output should be four binary signals: W, X, Y, Z (with weights 2, 4, 2, 1 respectively). • Treat all unused input combinations as don't-care conditions. Draw the combinational logic circuit that performs the required code conversion using logic gates.	15	3	4
3		An industrial fault-blocking controller supervises a machine and decides whether it should be blocked from operation (F = 0) under unsafe or abnormal conditions. The controller monitors four binary signals: An industrial fault-blocking controller supervises a machine and decides whether it should be blocked from operation (F = 0) under unsafe or abnormal conditions. The controller monitors four binary signals: The output F = 1 indicates operation permitted, while F = 0 indicates operation blocked. The controller blocks the machine (F = 0) under the following unsafe input combinations: • Emergency stop released but temperature unsafe • Emergency stop released, temperature unsafe, door closed. • Emergency stop released, temperature safe, door open. • Power ON while emergency stop engaged.	15	2	3

Variable	Logic 1
A	Main power supply is ON
B	Emergency stop is released
C	Operating temperature is within safe limit
D	Safety enclosure door is closed

		• Power ON, emergency stop engaged, door closed The following input combinations never arise due to hardware enforcement and supervisory control, and therefore the output of this controller is irrelevant for these states: Complete shutdown / maintenance state. • Emergency stop engaged while all other safety signals active (physically impossible). • All systems active; control transferred to higher-level controller. (a) Minimize the function using the Quine–McCluskey procedure. (10 Marks) (b) Draw the logic circuit using basic Gates. (5 Marks).	
4		Design a combinational circuit with three inputs x, y and z and the 3 outputs, A, B, and C. When the binary input is 0, 1, 2 or 3 the binary output is one greater than the input. When the binary input is 4, 5, 6 or 7, the binary output is one less than the input.	5

**********All the best **********